GENERAL DESCRIPTION

The SGM40657/8 over-voltage protection devices feature a low 20mΩ (TYP) $R_{ON}$ internal FET and protect low-voltage systems against voltage faults up to +28V DC. An internal clamp also protects the devices from surges up to +120V. When the input voltage exceeds the over-voltage threshold, the internal FET is turned off to prevent damage to the protected downstream components.

The over-voltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. If the OVLO input is below the external OVLO select voltage, the SGM40657/8 automatically choose the internal trip thresholds. The internal over-voltage thresholds ($V_{IN,OVLO}$) are preset to be 6.82V/5.95V typical (SGM40657/8). The devices feature an open-drain $ACOK$ output indicating a stable supply between minimum supply voltage and $V_{OVLO}$. The SGM40657/8 are also protected against over-current events by an internal thermal shutdown.

The SGM40657/8 are available in Green 12-Ball CSP package and operate over an ambient temperature range of -40°C to +85°C.

FEATURES

- Protect High-Power Portable Devices
  - Wide Operating Input Voltage Protection from 2.5V to 28V
  - Integrated 20mΩ (TYP) N-Channel MOSFET Switch
- Flexible Over-Voltage Protection Design
  - Adjustable Over-Voltage Protection Trip Level
  - Wide Adjustable OVLO Threshold Range from 4V to 20V
  - Internal Preset OVLO Thresholds:
    - 6.82V (SGM40657)
    - 5.95V (SGM40658)
- Additional Protection Features Increase System Reliability
  - Surge Immunity up to +120V
  - Soft-Start to Minimize In-Rush Current
  - Internal 15ms Startup Debounce
  - Thermal Shutdown Protection
- Enable Function
- -40°C to +85°C Operating Temperature Range
- Available in Green WLCSP-1.31×1.84-12B Package

APPLICATIONS

Smart Phones
Tablet PCs
Mobile Internet Devices
SGM40657/SGM40658 High-Current Over-Voltage Protector

PACKAGE/ORDERING INFORMATION

<table>
<thead>
<tr>
<th>MODEL</th>
<th>PACKAGE DESCRIPTION</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
<th>ORDERING NUMBER</th>
<th>PACKAGE MARKING</th>
<th>PACKING OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SGM40657</td>
<td>WLCSP-1.31×1.84-12B</td>
<td>-40°C to +85°C</td>
<td>SGM40657YG/TR</td>
<td>XXXXX GM3YG</td>
<td>Tape and Reel, 3000</td>
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<tr>
<td>SGM40658</td>
<td>WLCSP-1.31×1.84-12B</td>
<td>-40°C to +85°C</td>
<td>SGM40658YG/TR</td>
<td>XXXXX GM4YG</td>
<td>Tape and Reel, 3000</td>
</tr>
</tbody>
</table>

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOlute mAXIMUM RATINGS

IN (with respect to GND)...........................................-0.3V to 28V
IN (with respect to GND)...... +120V, 1.2/50μs, 2Ω surge
OUT (with respect to GND).................................-0.3V to VIN + 0.3V
OVLO .............................................................. -0.3V to 26.4V
ACOK , EN (with respect to GND)..............................-0.3V to 6V
Continuous IN, OUT Current .....................................6A
Peak IN, OUT Current (10ms) ...................................8A
Junction Temperature ...........................................+150°C
Storage Temperature Range ..............................-65°C to +150°C
Lead Temperature (Soldering 10 sec) ..................+260°C
ESD Susceptibility
HBM .........................................................................7kV
MM .............................................................................400V
CDM ..........................................................................1kV
Air Gap Discharge on IN Pin (IEC61000-4-2) ............20kV
Contact Discharge on IN Pin (IEC61000-4-2) ............12kV

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range..............................................2.5V to 28V
Operating Temperature Range..............................-40°C to +85°C

NOTES:
1. Non-frequent repeat peak voltage during input surge transient and ESD transient is not subject to this rating value, which may go higher than 35V during the surge test.
2. Surge test in compliance with IEC61000-4-5 specification.
3. Survives burst pulse up to +120V with 2Ω series resistance.
4. Continuous current limit may vary with the circuit board thermal dissipation condition.
5. If prote ction discharging triggered, the discharging keeps until the supply falls below the hysteresis range. Continuously force driving during discharging with a voltage in the hysteresis range would cause over stress or even damage the device. Supply voltage within the hysteresis range is not recommended. A 1kΩ resistor should be inserted in supply path for clamp voltage evaluation to avoid over stress damage by unintended triggering.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
PIN CONFIGURATION

SGM40657/8 (TOP VIEW)

WLCSP-1.31×1.84-12B

PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>EN</td>
<td>Enable Control. When ( \text{EN} = \text{Low} ), chip is enabled; when ( \text{EN} = \text{High} ), chip is in disable status.</td>
</tr>
<tr>
<td>A4, B4, C4</td>
<td>GND</td>
<td>Ground. Connect GND pins together for proper operation.</td>
</tr>
<tr>
<td>B1</td>
<td>ACOK</td>
<td>Open-Drain Flag Output. ( \text{ACOK} ) is driven low after input voltage is stable between minimum ( V_{\text{IN}} ) and ( V_{\text{OVLO}} ) after debounce. Connect a pull-up resistor from ( \text{ACOK} ) to the logic I/O voltage of the host system. ( \text{ACOK} ) is high impedance after thermal shutdown.</td>
</tr>
<tr>
<td>B3, C2, C3</td>
<td>IN</td>
<td>Input Voltage. Bypass IN with a 0.1μF ceramic capacitor as close as possible to the device. Connect IN pins together for proper operation.</td>
</tr>
<tr>
<td>C1</td>
<td>OVLO</td>
<td>External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.</td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS**

(V\textsubscript{IN} = 2.5V to 28V, \(E\text{N} = 0V\), \(C\text{IN} = 0.1\mu\text{F}\), \(T\text{A} = -40\degree\text{C} \text{ to } +85\degree\text{C}\), typical values are at \(V\text{IN} = 5V\), \(I\text{IN} \leq 3A\), \(T\text{A} = +25\degree\text{C}\), unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>(V\text{IN})</td>
<td>(\text{V})</td>
<td>2.5</td>
<td>28</td>
<td>28</td>
<td>(\text{V})</td>
</tr>
<tr>
<td>Input Clamp Triggering Voltage</td>
<td>(V\text{IN,CLAMP})</td>
<td>(I\text{IN} = 10\text{mA} \text{ limited, } T\text{A} = +25\degree\text{C})</td>
<td>28.8</td>
<td></td>
<td></td>
<td>(\text{V})</td>
</tr>
<tr>
<td>Input Clamp Hysteresis</td>
<td>(V\text{HYST})</td>
<td>(\text{V})</td>
<td>0.75</td>
<td></td>
<td></td>
<td>(\text{V})</td>
</tr>
<tr>
<td>Input Supply Current</td>
<td>(I\text{IN})</td>
<td>(V\text{IN} = 5\text{V})</td>
<td>95</td>
<td>155</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>OVLO Supply Current</td>
<td>(I\text{IN,Q})</td>
<td>(V\text{OVLO} = 3\text{V}, V\text{IN} = 5\text{V}, V\text{OUT} = 0\text{V})</td>
<td>95</td>
<td>155</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>(I\text{Q,OFF})</td>
<td>(V\text{IN} = 5\text{V}, E\text{N} = 2\text{V})</td>
<td>2</td>
<td></td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
</tbody>
</table>

| VBG Reference | \(V\text{BG}\) | | 1.180 | 1.216 | 1.255 | \(\text{V}\) |
| Adjustable OVLO Threshold Range | | | 4 | 20 | | \(\text{V}\) |
| External OVLO Select Threshold | \(V\text{OVLO,SELECT}\) | | 0.23 | 0.26 | 0.30 | \(\text{V}\) |
| Switch On-Resistance | \(R\text{ON}\) | \(V\text{IN} = 5\text{V}, I\text{OUT} = 0.5\text{A}, T\text{A} = +25\degree\text{C}\) | 20 | 35 | | \(\text{m}\Omega\) |
| OUT Load Capacitance | \(C\text{OUT}\) | \(V\text{IN} = 5\text{V}\) | 1000 | | | \(\mu\text{F}\) |
| IN Leakage Voltage by OVLO | \(V\text{IN,LEAK}\) | \(V\text{OVLO} = 20\text{V}, V\text{IN} = \text{unconnected, } R\text{OVLO} = 1\text{M}\Omega\) | 0.2 | | | \(\text{V}\) |
| Thermal Shutdown | | | 150 | | | \(\degree\text{C}\) |
| Thermal Shutdown Hysteresis | | | 30 | | | \(\degree\text{C}\) |

**DIGITAL SIGNAL (\(\text{ACOK}\))**

| \(\text{ACOK}\) Output Low Voltage | \(V\text{OL}\) | \(V\text{OL} = 3.3\text{V, } I_{\text{ISINK}} = 1\text{mA, See Figure 1}\) | 0.26 | 0.32 | | \(\text{V}\) |
| \(\text{ACOK}\) Leakage Current | \(I_{\text{ACOK,LEAK}}\) | \(V\text{OL} = 3.3\text{V, } \text{ACOK }\text{ deasserted, See Figure 1}\) | 1 | | | \(\mu\text{A}\) |

**TIMING CHARACTERISTICS**

| Debounce Time | \(t\text{DEB}\) | Time from \(V\text{IN} > 2.5\text{V}\) to the time \(V\text{OUT}\) starts rising | 15 | | | \(\text{ms}\) |
| Soft-Start Time | \(t\text{SS}\) | Time from \(V\text{IN} > 2.5\text{V}\) to soft-start off | 30 | | | \(\text{ms}\) |
| Switch Turn-On Time | \(t\text{ON}\) | \(V\text{IN} = 5\text{V}, R\text{R} = 100\Omega, C\text{LOAD} = 100\mu\text{F, VOUT from }10\%\text{, VIN to }90\%\text{ VIN}\) | 1.5 | | | \(\text{ms}\) |
| Switch Turn-Off Time | \(t\text{OFF}\) | \(V\text{IN} > V\text{IN,OVLO to }V\text{OUT} = 80\%\text{ of }V\text{IN, }R\text{R} = 100\Omega, \text{with }20\%\text{ over drive, for the case of using the internal threshold}\) | 50 | | | \(\text{ns}\) |
| Switch Turn-Off Propagation Delay | \(t\text{DELAY}\) | \(V\text{OVLO} > V\text{BG} \text{ with }20\%\text{ over drive to output falling }10\%, R\text{R} = 100\Omega. \text{For the case of using external threshold}\) | 80 | | | \(\text{ns}\) |

**\(E\text{N}\) LOGIC LEVELS**

| Logic LOW Input Voltage | \(V\text{L}\) | | 0.4 | | | \(\text{V}\) |
| Logic HIGH Input Voltage | \(V\text{H}\) | | 1.6 | | | \(\text{V}\) |
| \(E\text{N}\) Leakage Current | \(I_{\text{EN,LEAK}}\) | \(V\text{IN} = 5\text{V}\) | 1 | | | \(\mu\text{A}\) |
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5V$, $EN = 0V$, $C_{IN} = 0.1\mu F$, $C_{OUT} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

**Input Supply Current vs. Input Voltage**

**OVLO Leakage Current vs. OVLO Pin Voltage**

**Normalized On-Resistance vs. Output Current**

$R_{ON} = 20m\Omega$ (TYP)

**Normalized OVLO Threshold vs. Temperature**

Normalized to $T_A = +25^\circ C$

**Normalized External OVLO Select Threshold vs. Temperature**

$V_{IN} = 2.5V$

Normalized to $T_A = +25^\circ C$

**Normalized External OVLO Select Threshold vs. Temperature**

$V_{IN} = 28V$

Normalized to $T_A = +25^\circ C$
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Vin = 5V, EN = 0V, Cin = 0.1μF, Cout = 1μF, TA = +25°C, unless otherwise noted.

Normalized On-Resistance vs. Temperature

Over-Voltage Fault Response

Power-Up Response

Power-Up Response

IN-GND 120V Surge Discharge Waveforms
(On-State)

IN-GND 120V Surge Discharge Waveforms
(Off-State)
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Vin = 5V, EN = 0V, Cin = 0.1μF, Cout = 1μF, TA = +25°C, unless otherwise noted.

Open Circuit Voltage Waveform without SGM40657/8, +120V, 1.2/50μs Surge

Vin

200μs/div

Time (20μs/div)

20V/div
SGM40657/SGM40658 High-Current Over-Voltage Protector

TYPICAL APPLICATION

* R₁ and R₂ are only required for adjustable OVLO; otherwise, connect OVLO to GND.

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

Figure 2. Block Diagram
TIMING DIAGRAM

NOTE: Waveforms are not to scale.

Figure 3. Timing Diagram

SURGE UP TEST CIRCUIT

Surge Generator in Compliance with IEC61000-4-5 Specification

5V Power Supply

Figure 4. Surge Up Test Circuit
DETAILED DESCRIPTION

The SGM40657/8 over-voltage protection devices feature a low on-resistance ($R_{ON}$) internal FET and protect low-voltage systems against voltage faults up to $+28\text{V}_{\text{DC}}$. An internal clamp also protects the devices from surges up to $+120\text{V}$. Surge up tests are operated according to the test circuit in Figure 4. If the input voltage exceeds the over-voltage threshold, the internal FET is turned off to prevent damage to the protected components. A 15ms (TYP) debounce time built into the device prevents false turn-on of the internal FET during startup.

Device Operation
The devices contain timing logic that controls the turn-on of the internal FET. The internal charge pump is enabled when $V_{\text{IN}} < V_{\text{IN,OVLO}}$, if internal trip thresholds are used or when $V_{\text{OVLO}} < V_{\text{OVLO,EXT}}$ if external trip thresholds are used. The charge-pump after a 15ms (TYP) debounce delay, turns the internal FET on (see Figure 2). After the debounce time, soft-start limits the FET inrush current for 15ms (TYP). At any time, if $V_{\text{IN}}$ rises above $V_{\text{OVLO,THRESH}}$, OUT is disconnected from IN.

Enable Function
The IC has an enable pin which is used to enable or disable the device. Connect the $\overline{\text{EN}}$ pin high to turn off the internal pass FET. Connect the $\overline{\text{EN}}$ pin low to turn on the internal pass FET and enter the start-up routine.

Internal Switch
The SGM40657/8 incorporate an internal FET with a 20m$\Omega$ (TYP) $R_{ON}$. The FET is internally driven by a charge pump that generates a necessary gate voltage above IN.

Over-Voltage Lockout (OVLO)
The SGM40657/8 have $6.82\text{V}/5.95\text{V}$ (TYP) over-voltage threshold (OVLO) respectively.

Thermal Shutdown Protection
The SGM40657/8 feature thermal shutdown circuitry. The internal FET turns off when the junction temperature exceeds $150^\circ\text{C}$ (TYP). The device exits thermal shutdown after the junction temperature cools by $30^\circ\text{C}$ (TYP).

$\overline{\text{ACOK}}$ Output
An open-drain $\overline{\text{ACOK}}$ output gives the SGM40657/8 the ability to communicate a stable power source to the host system. $\overline{\text{ACOK}}$ is driven low after input voltage is stable between minimum $V_{\text{IN}}$ and $V_{\text{OVLO}}$ after debounce. Connect a pull-up resistor from $\overline{\text{ACOK}}$ to the logic I/O voltage of the host system. $\overline{\text{ACOK}}$ is high impedance after thermal shutdown.

USB OTG Support
When used in an OTG application the SGM40657/8 can provide power from OUT to IN. Initially, the OTG voltage applied at OUT will forward-bias the power switch bulk diode and present a voltage drop of approximately 0.7V between OUT and IN. Once the voltage at IN exceeds the minimum input voltage of 2.5V and the debounce time has elapsed, the main power switch will turn fully on, significantly reducing the voltage drop from OUT to IN. In this mode, the part is able to supply a continuous current up to 3.5A to the OTG load.
APPLICATION INFORMATION

Bypass Capacitor
For most applications, bypass IN to GND with a 0.1\(\mu\)F ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, the device clamps the overshoot due to LC tank circuit.

Output Capacitor
The slow turn-on time provides a soft-start function that allows the SGM40657/8 to charge an output capacitor up to 1000\(\mu\)F without turning off due to an over-current condition.

Enhancing Surge Absorbability
When the input voltage ramps higher than the \(V_{\text{IN,CLAMP}}\), it triggers an active path in the device to discharge the input quickly until the input voltage falls \(V_{\text{HY}}\) below the \(V_{\text{IN,CLAMP}}\). Input rising and discharging may repeat until the surge source energy is discharged. A voltage pulse with saw shape top is clamped between the \(V_{\text{IN,CLAMP}}\) and the active path's resumable breaking voltage, which protects components which are connected to the device's input or output.

As the active path tries to pull in more energy upon triggering, only those absorption components with similar triggering voltage and similar residual voltage could share their capability for enhancing surge absorption. Both the trigger voltage and the residual voltage should be evaluated for selection matched companion absorption components. As a rule of thumb, a TVS with triggering voltage lower than the \(V_{\text{IN,CLAMP}}\) is recommended.

External OVLO Adjustment Functionality
The device detects voltage at the OVLO pin to check if an external divider exists. If OVLO is connected to ground, the internally set OVLO value will be applied.

If an external resistor-divider is connected to OVLO and \(V_{\text{OVLO}}\) exceeds the OVLO select voltage, \(V_{\text{OVLO,SELECT}}\), then this external resistor divider determines the \(V_{\text{IN,OVLO,EXT}}\). \(R_1 = 1\Omega\) is a good starting value for minimum current consumption. Since \(V_{\text{IN,OVLO,EXT}}, V_{BG}\), and \(R_1\) are known, \(R_2\) can be calculated from the following formula:

\[
V_{\text{IN,OVLO,EXT}} = V_{BG} \times \left[1 + \frac{R_1}{R_2}\right]
\]

This external resistor-divider is completely independent from the internal resistor-divider.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2017) to REV.A
Changed from product preview to production data
PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS

WLCSP-1.31×1.84-12B

NOTE: All linear dimensions are in millimeters.
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Reel Diameter</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P0 (mm)</th>
<th>P1 (mm)</th>
<th>P2 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>WLCSP-1.31×1.84-12B</td>
<td>7&quot;</td>
<td>9.2</td>
<td>1.40</td>
<td>2.00</td>
<td>0.80</td>
<td>4.0</td>
<td>4.0</td>
<td>2.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>
CARTON BOX DIMENSIONS

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

<table>
<thead>
<tr>
<th>Reel Type</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
<th>Pizza/Carton</th>
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</thead>
<tbody>
<tr>
<td>7&quot; (Option)</td>
<td>368</td>
<td>227</td>
<td>224</td>
<td>8</td>
</tr>
<tr>
<td>7&quot;</td>
<td>442</td>
<td>410</td>
<td>224</td>
<td>18</td>
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