

### GENERAL DESCRIPTION

The SGM61450 is a current mode controlled non-synchronous Buck converter with 4.5V to 42V input range and 5A continuous output current. A low  $R_{DS(ON)}$  N-MOSFET is integrated as high-side switch. The quiescent current is as low as 148 $\mu$ A. The shutdown current drops to 2.75 $\mu$ A during shutdown (EN = low). The internal under-voltage lockout (UVLO) threshold is 4.2V and can be adjusted (increased) by an external resistor divider. An internal soft-start circuit controls the output voltage start-up ramp. Switching frequency can be selected over a wide range (100kHz to 2500kHz) to allow desired tradeoff among efficiency, component sizes and conversion voltage ratio. Protection against over-voltage transient is provided to limit the startup or other transient overshoots. Secure operation in overload conditions is ensured by cycle-by-cycle current limit, frequency fold-back and thermal shutdown protection.

The SGM61450 is available in a Green SOIC-8 (Exposed Pad) package.

### FEATURES

- 4.5V to 42V Input Voltage Range
- 0.8V to 36V Adjustable Output Voltage Range
- Integrated 68m $\Omega$  High-side MOSFET Supports up to 5A Continuous Output Current
- Programmable Switching Frequency: 100kHz to 2500kHz
- Low Quiescent Current: 148 $\mu$ A (TYP)
- Low Shutdown Current: 2.75 $\mu$ A (TYP)
- Power-Save Mode for High Light Load Efficiency
- Frequency Synchronization to External Clock
- Programmable UVLO Threshold
- Over-Voltage Transient Protection
- Cycle-by-Cycle Current Limit
- Frequency Fold-Back Protection
- Integrated BOOT Recharge FET for Low Light Load Dropout
- Thermal Shutdown (+176 $^{\circ}$ C)
- Available in a Green SOIC-8 (Exposed Pad) Package

### APPLICATIONS

- USB Dedicated Charging Ports
- Industrial Power Supplies
- Battery Chargers

### TYPICAL APPLICATION

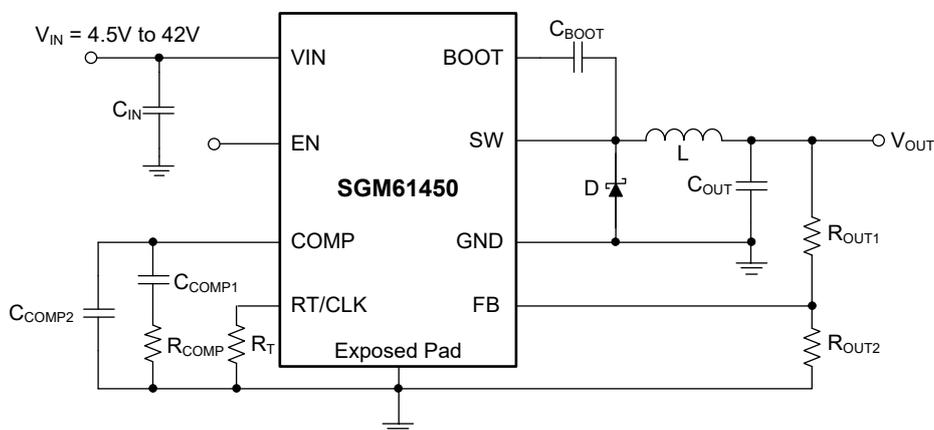


Figure 1. Typical Application Circuit

## PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61450	SOIC-8 (Exposed Pad)	-40°C to +125°C	SGM61450XPS8G/TR	SGM 61450XPS8 XXXXX	Tape and Reel, 4000

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

**XXXXX**



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Input Voltages (Referred to GND Pin if not Specified)

V <sub>IN</sub> .....	-0.3V to 45V
EN .....	-0.3V to 45V
FB .....	-0.3V to 3V
COMP .....	-0.3V to 3V
RT/CLK .....	-0.3V to 5.5V

Output Voltages

BOOT to SW .....	6V
SW to GND .....	-0.6V to 45V
SW to GND (10ns Transient) .....	-2V to 45V

Package Thermal Resistance

SOIC-8 (Exposed Pad), $\theta_{JA}$ .....	40°C/W
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Junction Temperature .....

.....	+150°C
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Storage Temperature Range .....

.....	-65°C to +150°C
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Lead Temperature (Soldering, 10s) .....

.....	+260°C
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ESD Susceptibility

HBM .....	2500V
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CDM .....	1000V
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## RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage, V<sub>IN</sub> .....

.....	4.5V to 42V
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Output Voltage, V<sub>O</sub> .....

.....	0.8V to 36V
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Output Current, I<sub>O</sub> .....

.....	0A to 5A
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Operating Junction Temperature Range .....

.....	-40°C to +125°C
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## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

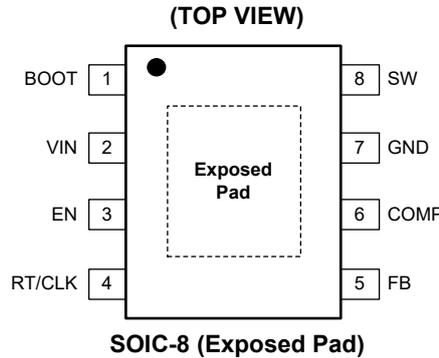
## ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	BOOT	P	Bootstrap Input (for N-MOSFET Gate Driver Supply Voltage). Connect this pin to SW pin with a 0.1μF ceramic capacitor. The high-side MOSFET will be turned off if the BOOT capacitor voltage drops below its BOOT-UVLO level to get the capacitor voltage refreshed.
2	VIN	P	Supply Input. Connect to a 4.5V to 42V power source.
3	EN	I	Active High Enable Input. Float or pull up to enable or pull down below 1.18V to disable the device. Input UVLO threshold can be programmed using a resistor divider from VIN pin.
4	RT/CLK	I	Frequency Setting Resistor (RT) or External SYNC Clock Input Pin. The voltage on this pin is kept at a constant level by an internal amplifier for setting frequency by the external RT resistor. If an external clock signal is connected to this pin, it will act as a synchronization input and the switching frequency will be synchronized to external clock. When the clock stops (no clock) and no fast transient edges are detected, the internal amplifier will be enabled again and the pin returns to RT mode (resistor frequency setting).
5	FB	I	Feedback Input. FB is the inverting input of the control loop transconductance (gm) error amplifier (EA). It is used as the feedback input to sense and regulate V <sub>OUT</sub> . Connect a feedback resistor divider tap to this pin.
6	COMP	O	EA Output (internally connected to the PWM comparator input). Place the compensation network between COMP and GND pins. The EA output current is injected into this network to create the control voltage (V <sub>COMP</sub> ). It will be compared with the compensated sensed current signal to generate the switching pulses (set duty cycle).
7	GND	G	Ground Pin.
8	SW	P	Switching Node. It is connected to the source of the internal high-side switch. An external switching power diode (catch diode) must be connected between this pin (cathode) and GND (anode) to complete the Buck converter.
—	Exposed Pad	G	Exposed Pad. This pin must be connected directly to the GND pin and is intended for better device cooling by providing a low thermal resistance path from junction to the PCB.

NOTE: I = input, O = output, G = ground, P = power.

## ELECTRICAL CHARACTERISTICS

(T<sub>J</sub> = -40°C to +125°C, V<sub>IN</sub> = 4.5V to 42V, typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.)

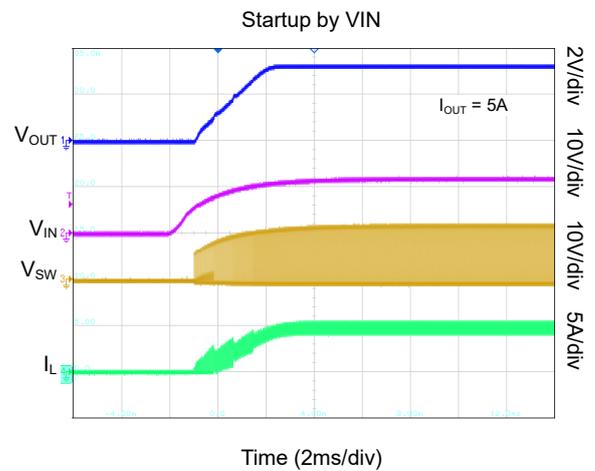
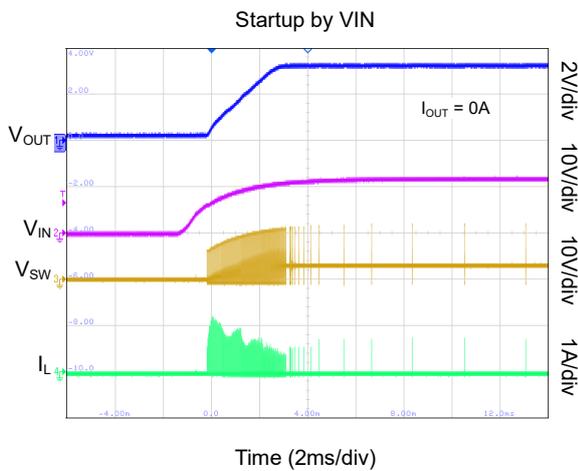
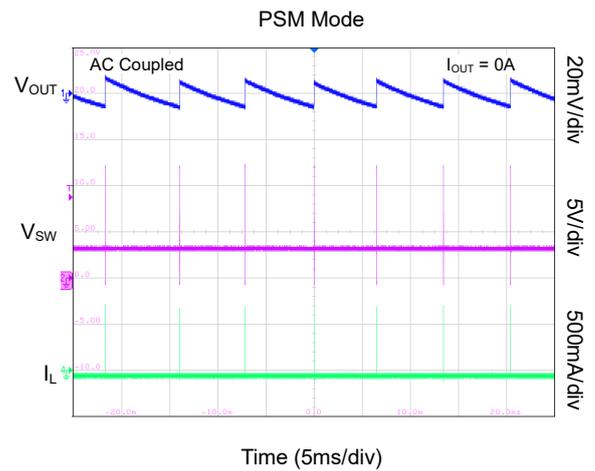
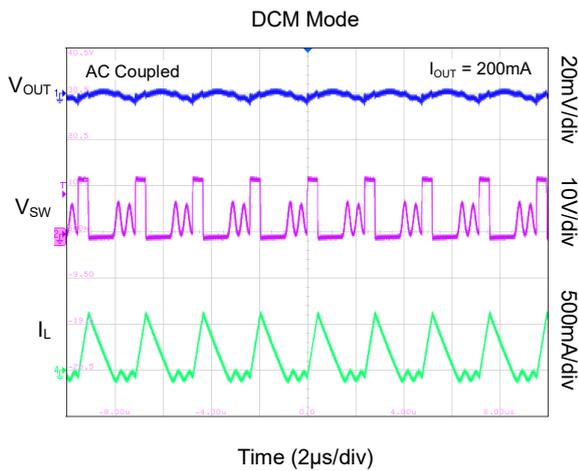
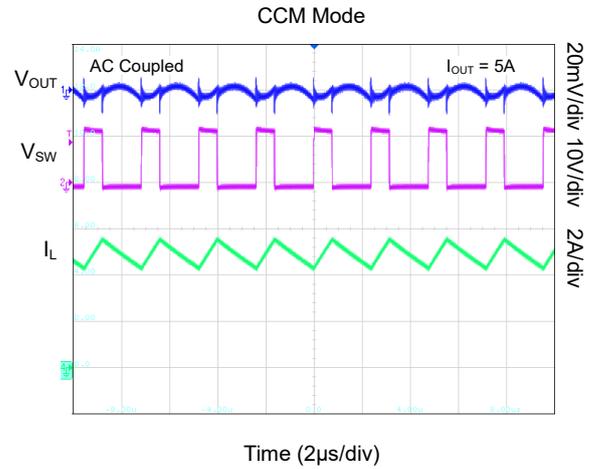
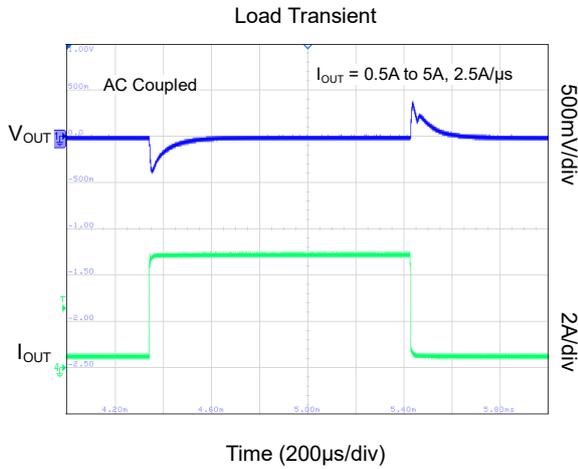
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Voltage (VIN Pin)</b>						
Operating Input Voltage	V <sub>IN</sub>		4.5		42	V
Under-Voltage Lockout Threshold	V <sub>UVLO</sub>	V <sub>IN</sub> rising	4.0	4.2	4.5	V
Under-Voltage Lockout Threshold Hysteresis	V <sub>UVLO_HYS</sub>			270		mV
Shutdown Current	I <sub>SD</sub>	T <sub>J</sub> = +25°C, V <sub>EN</sub> = 0V		2.75	6.6	μA
Quiescent Current (No Switching)	I <sub>Q</sub>	T <sub>J</sub> = +25°C, V <sub>FB</sub> = 0.9V		148	175	μA
<b>Enable and UVLO (EN Pin)</b>						
Enable Threshold Voltage	V <sub>EN_TH</sub>	Rising and falling (there is no hysteresis)	1.1	1.18	1.3	V
EN Input Current (Negative Value Means Current Going out of the IC)	I <sub>EN</sub>	Enable threshold +50mV (I <sub>EN2</sub> )		-4.8		μA
		Enable threshold -50mV (I <sub>EN1</sub> )	-0.8	-1.3	-1.8	
Internal Current Source Hysteresis Current	I <sub>EN_HYS</sub>		-2.7	-3.5	-4.1	μA
<b>Voltage Reference</b>						
Internal Voltage Reference	V <sub>FB</sub>		0.789	0.8	0.824	V
<b>High-side Internal MOSFET (High-side)</b>						
On-Resistance	R <sub>DS(on)</sub>	V <sub>IN</sub> = 12V, V <sub>BOOT</sub> - V <sub>SW</sub> = 5V		68	130	mΩ
<b>Error Amplifier (EA)</b>						
Input Current (FB pin)	I <sub>IN</sub>			10		nA
Error Amplifier DC Voltage Gain	A <sub>EA</sub>	V <sub>FB</sub> = 0.8V		10000		V/V
Unity-Gain Bandwidth				2500		kHz
EA Amp Source/Sink Current	I <sub>EA</sub>	V <sub>FB</sub> = 0.7V/0.9V		±30		μA
SW Current to V <sub>COMP</sub> Transconductance	g <sub>mps</sub>			14		A/V
Error Amplifier Transconductance (gm)	G <sub>EA</sub>	-2μA < I <sub>COMP</sub> < 2μA, V <sub>COMP</sub> = 1V		407		μs
Error Amplifier Transconductance (gm) during Soft-Start	G <sub>EA_SS</sub>	-2μA < I <sub>COMP</sub> < 2μA, V <sub>COMP</sub> = 1V, V <sub>FB</sub> = 0.4V		77		μs
<b>Switch Current Limit</b>						
Open-Loop Current-Limit (Directly Tested and Measured at the SW Pin, Independent of the Inductance or Slope Compensation)	I <sub>LIMIT</sub>	V <sub>IN</sub> = 4.5V to 42V	6.2	8.0	9.95	A
		V <sub>IN</sub> = 12V	6.2	8.0	9.95	
		T <sub>J</sub> = +25°C, V <sub>IN</sub> = 12V	6.7	8.0	9.45	
<b>Thermal Shutdown</b>						
Thermal Shutdown	T <sub>SHDN</sub>	Temperature rising		176		°C
Thermal Shutdown Hysteresis	T <sub>HYS</sub>			20		°C
<b>Timing Resistor (R<sub>T</sub>) and External SYNC Clock (RT/CLK Pin)</b>						
Switching Frequency Range at RT Mode	f <sub>SW</sub>		100		2500	kHz
Switching Frequency Tolerance	f <sub>SW</sub>	R <sub>T</sub> = 200kΩ	450	500	550	kHz
SYNC Switching Frequency Range at CLK Mode	f <sub>CLK</sub>		160		2300	kHz
SYNC Input Clock High Level	V <sub>SYNC_R</sub>		1.9			V
SYNC Input Clock Low Level	V <sub>SYNC_F</sub>				0.9	V

## TIMING PARAMETERS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Enable and UVLO (EN Pin)</b>						
Device Enabled to COMP Active Delay		$T_J = +25^\circ\text{C}$ , $V_{IN} = 12\text{V}$		340		$\mu\text{s}$
<b>Internal Soft-Start Time</b>						
Soft-Start Time	$t_{SS}$	$f_{SW} = 500\text{kHz}$ , 0 to 100% reference voltage		2.73		ms
		$f_{SW} = 2500\text{kHz}$ , 0 to 100% reference voltage		0.546		ms
<b>Current Limit</b>						
Current-Limit Threshold Delay				60		ns
<b>Timing Resistor and External Clock (RT/CLK Pin)</b>						
Minimum CLK Input Pulse Width	$t_{CLK\_MIN}$			15		ns
RT/CLK Falling Edge to SW Rising Edge Delay		Measured at 500kHz with RT resistor in connected		70		ns
PLL Lock in Time	$t_{LOCK\_IN}$	Measured at 500kHz		78		$\mu\text{s}$

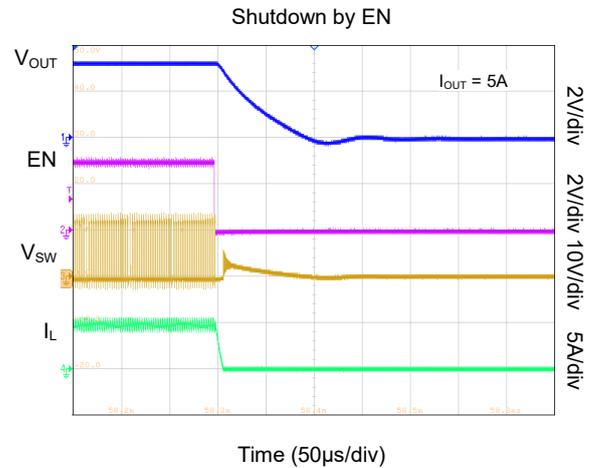
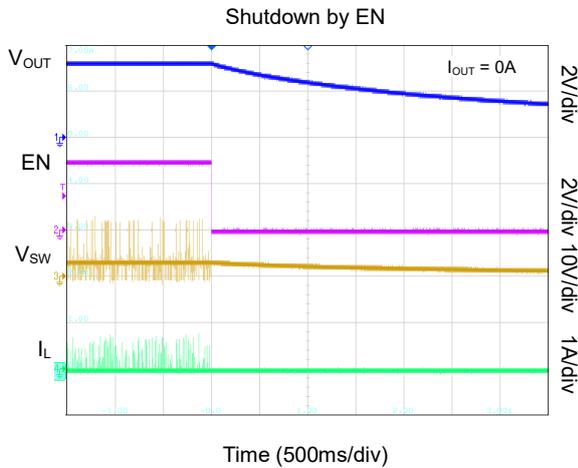
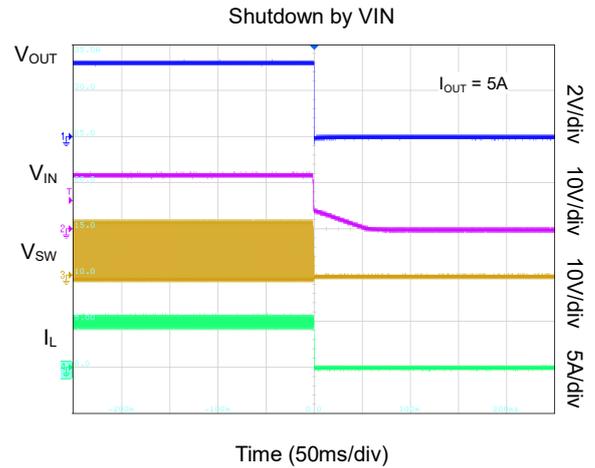
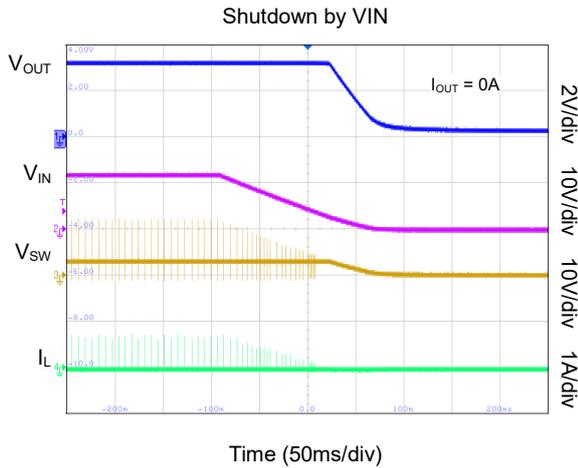
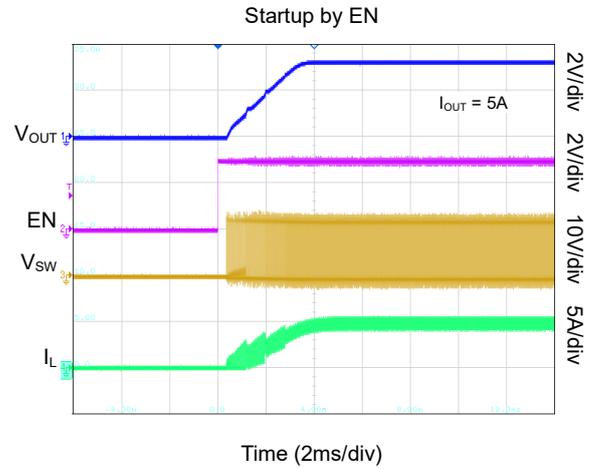
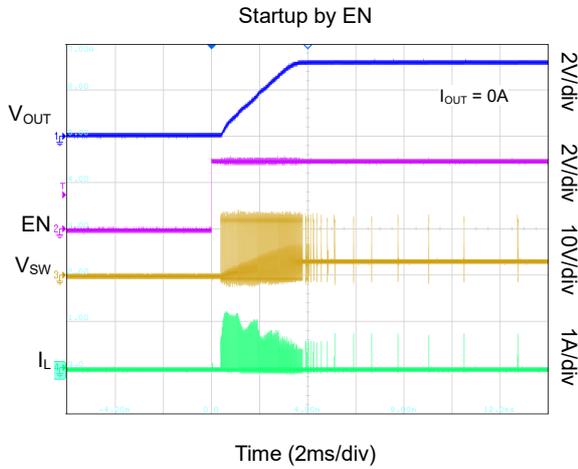
TYPICAL PERFORMANCE CHARACTERISTICS

T<sub>A</sub> = +25°C, V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 3.3V, f<sub>SW</sub> = 420kHz, L = 5.5µH and C<sub>OUT</sub> = 200µF, unless otherwise noted.



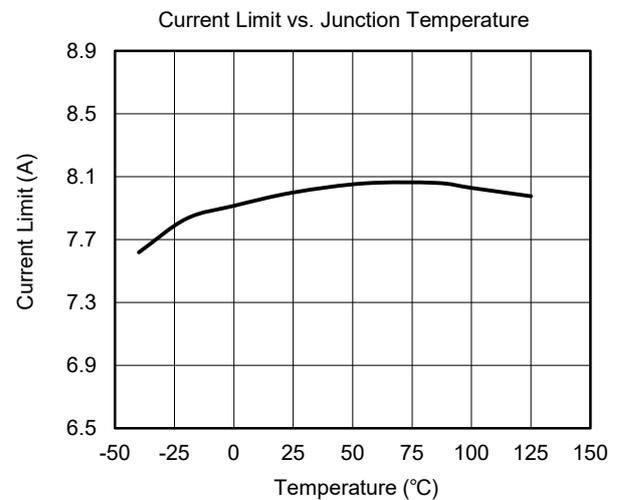
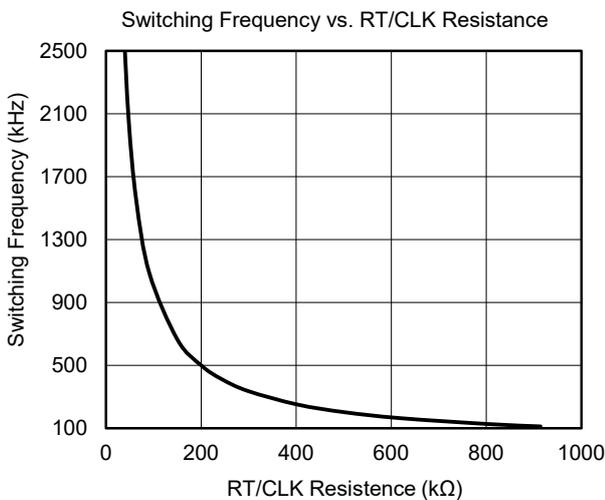
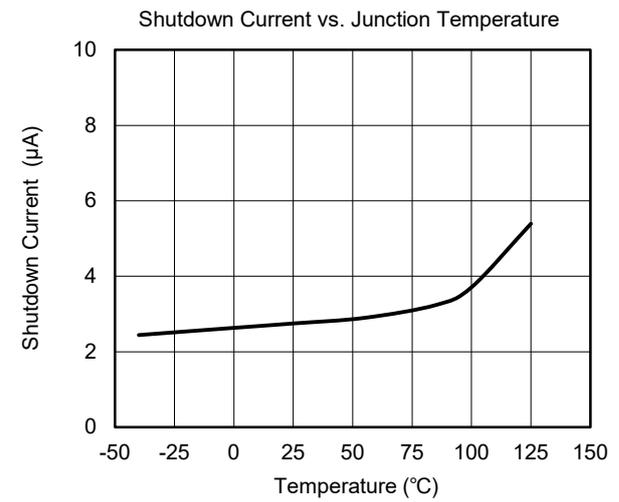
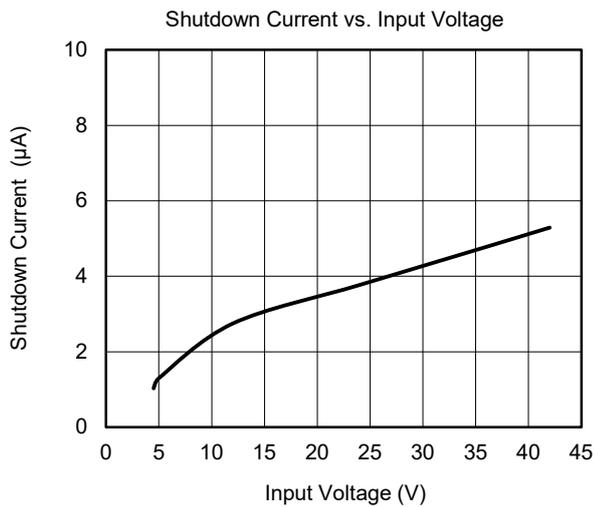
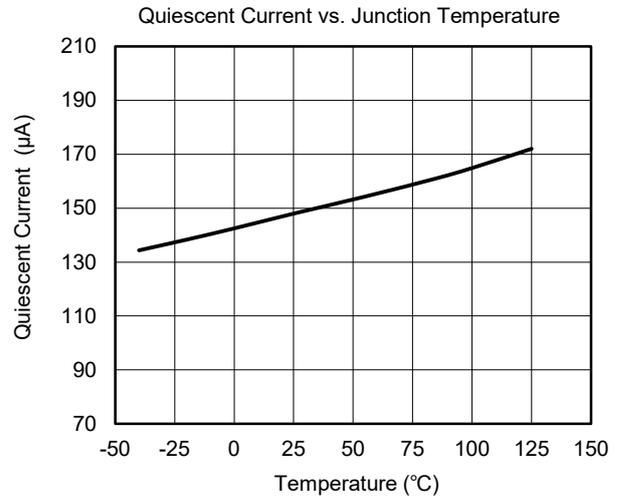
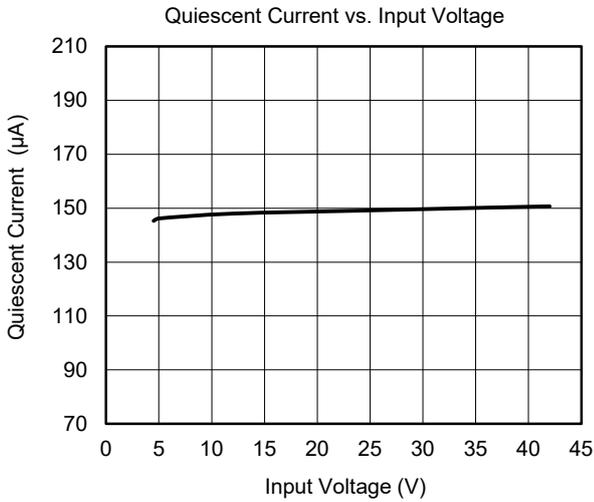
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T<sub>A</sub> = +25°C, V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 3.3V, f<sub>SW</sub> = 420kHz, L = 5.5μH and C<sub>OUT</sub> = 200μF, unless otherwise noted.



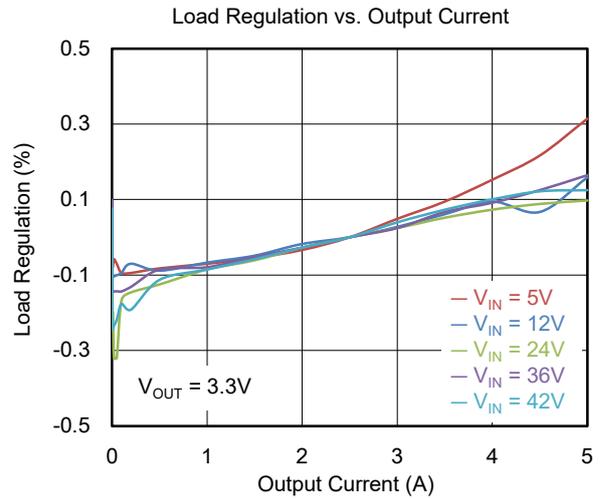
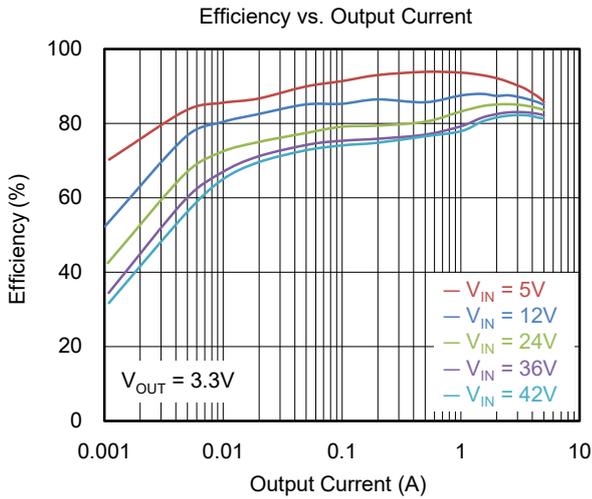
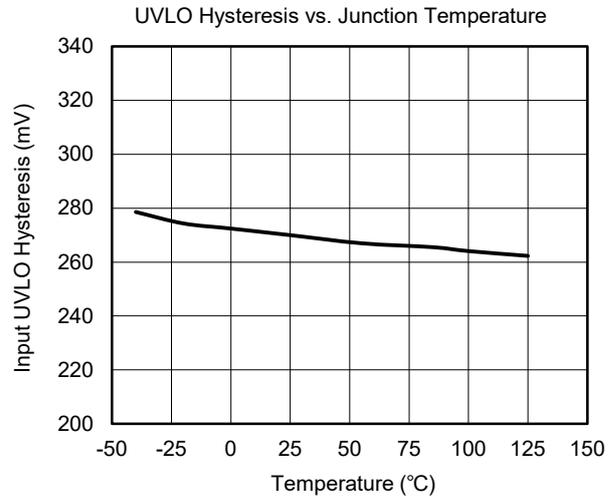
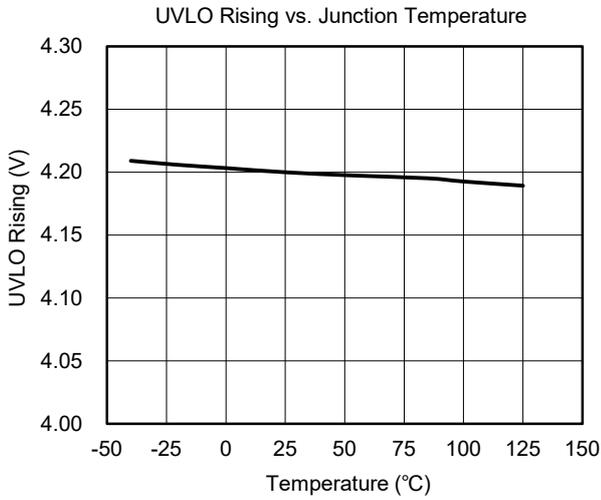
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T<sub>A</sub> = +25°C, V<sub>IN</sub> = 12V, f<sub>sw</sub> = 420kHz, L = 5.5µH and C<sub>OUT</sub> = 200µF, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

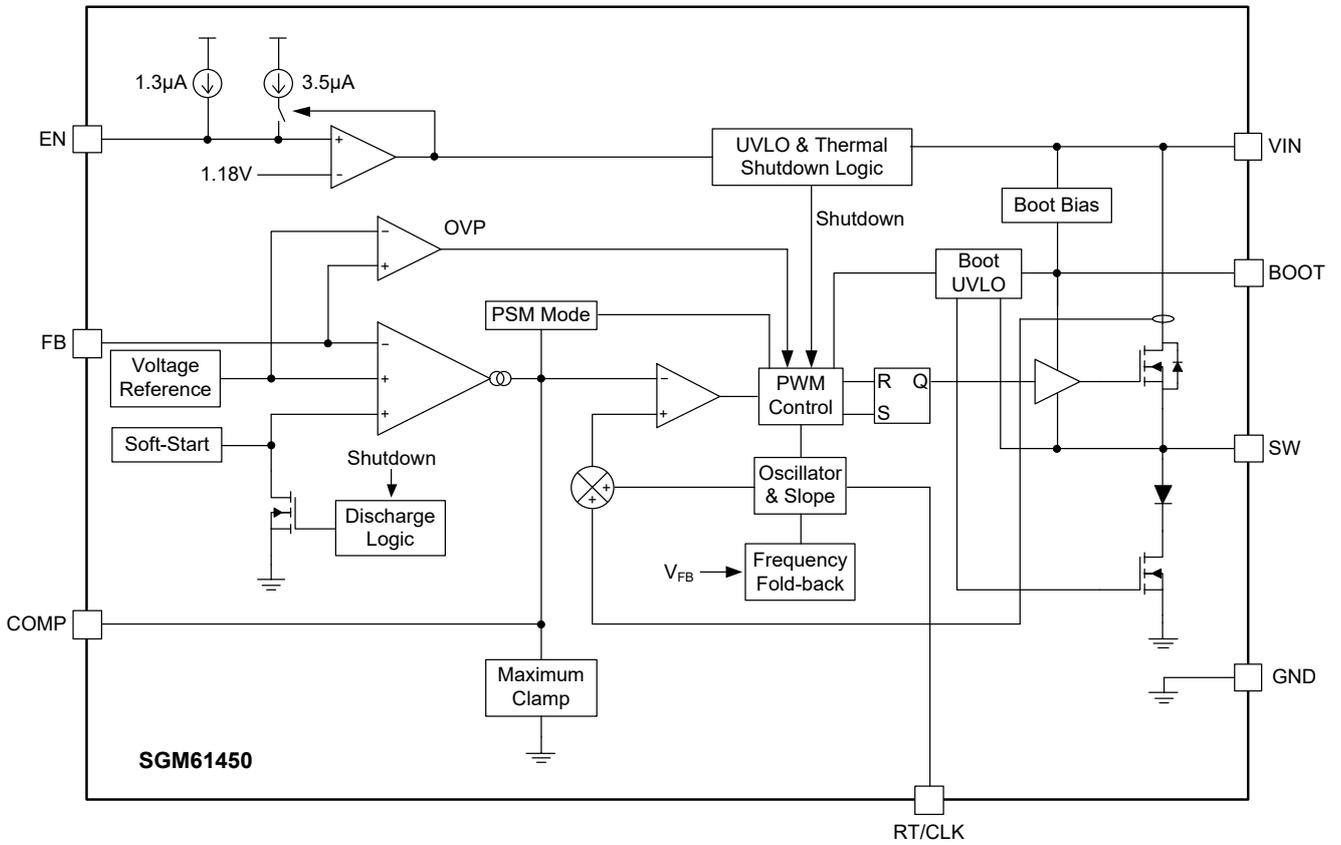


Figure 2. Block Diagram

## DETAILED DESCRIPTION

### Overview

The SGM61450 is a 42V Buck converter with integrated N-MOSFET power switch and 5A continuous output current capability. Using peak current mode control and operating at fixed PWM frequency, this device provides good line and load transient responses with reduced output capacitance.

The minimum operating input voltage of the device is 4.5V. The output voltage can be set down to 0.8V (reference voltage). The quiescent current is 148 $\mu$ A and shutdown current drops to 2.75 $\mu$ A during shutdown (EN = low). The low  $R_{\text{DS(ON)}}$  (68m $\Omega$ ) high-side switch allows high operating efficiency.

The EN pin is internally pulled up by a current source that can keep the device enable if EN is floating. It can also be used to increase the input UVLO threshold using a resistor divider.

This device can operate with duty cycles close to 100% using the automated internal  $C_{\text{BOOT}}$  recharge circuit. This feature allows setting the  $V_{\text{OUT}}$  very close to the  $V_{\text{IN}}$ .

The internal phase-locked loop (PLL) synchronizes to the RT/CLK pin so that the high-side switch turn-on time is synchronized to the input clock falling edges.

Over-voltage protection (OVP) circuit is designed to minimum the output over-voltage transients. When this comparator detects an OVP ( $V_{\text{FB}} > 109\% \times V_{\text{REF}}$ ), the switch is kept off until the output falls below 106% of the  $V_{\text{REF}}$ .

The output voltage ramps up slowly during start-up with slow increasing of the PWM reference voltage by the integrated soft-start circuit. Soft-start is necessary to limit the inrush current, output voltage overshoot and to avoid potential over-current hiccups during power-up. Any recovery from shutdown state begins with a soft-start.

Light load efficiency is enhanced by a special power-save mode that is activated when the peak inductor current falls below 690mA (TYP).

During startup and over-current, the frequency is reduced (frequency fold-back) to allow easy maintenance of low inductor current. The thermal shutdown provides an additional protection in fault conditions.

### Minimum Input Voltage (4.5V) and UVLO

The recommended minimum operating input voltage is 4.5V. The device may operate with lower voltages that are above the input UVLO threshold (4.2V TYP). If  $V_{\text{IN}}$  falls below its falling UVLO threshold, the device will stop switching.

### Enable Input and UVLO Adjustment

The device will be enabled if  $V_{\text{IN}}$  exceeds 4.2V and EN voltage is above 1.18V. The device will be disabled if the EN voltage is externally pulled low or the  $V_{\text{IN}}$  pin voltage falls below its UVLO threshold. When the EN pin is floating, an internal pull-up current source keeps the EN pin voltage at high state that enables the device.

If an application requires a higher input UVLO threshold, an external input UVLO adjustment circuit (resistor divider) is recommended in Figure 3. Figure 3 shows how UVLO and hysteresis are increased using  $R_{\text{EN1}}$  and  $R_{\text{EN2}}$ . A 3.5 $\mu$ A additional current is injected to the divider when EN pin voltage exceeds 1.18V to provide hysteresis. When the EN pin voltage falls below 1.18V, the 3.5 $\mu$ A additional current is removed. Use Equations 1 and 2 to calculate these resistors.  $V_{\text{START}}$  is the input start (turn-on) threshold voltage and  $V_{\text{STOP}}$  is the input stop (turn-off) threshold voltage.

$$R_{\text{EN1}} = \frac{V_{\text{START}} - V_{\text{STOP}}}{3.5\mu\text{A}} \quad (1)$$

$$R_{\text{EN2}} = \frac{V_{\text{EN}}}{\frac{V_{\text{START}} - V_{\text{EN}} + 1.3\mu\text{A}}{R_{\text{EN1}}}} \quad (2)$$

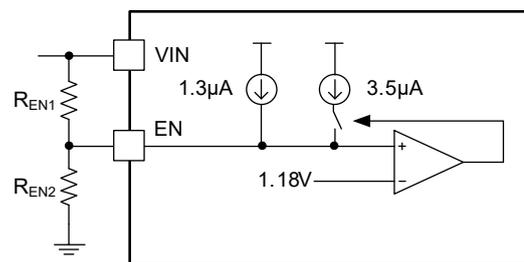


Figure 3. Input UVLO Adjustment

## DETAILED DESCRIPTION (continued)

### Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency can be set from 100kHz to 2500kHz by a timing resistor ( $R_T$ ) placed between the RT/CLK and GND pins. There is an internal bias voltage (0.5V TYP) on the RT/CLK pin during the RT mode and must have a resistor to ground to set the switching frequency. Use Equation 3 to find the  $R_T$  resistance for any desired switching frequency ( $f_{sw}$ ).

$$f_{sw} \text{ (kHz)} = \frac{92417}{R_T \text{ (k}\Omega\text{)}^{0.985}} \quad (3)$$

### Synchronization to RT/CLK Pin

The internal oscillator can synchronize to an external logic clock source applied to the RT/CLK pin (see Figure 4) in the 160kHz to 2300kHz range. The SW rising edge (high-side switch turn-on) is synchronized to the external logic clock falling edge. The external logic clock low and high levels must be less than 0.9V and more than 1.9V and have a pulse width larger than 15ns. So, when the external logic clock source is off, the DC resistance ( $R_T$ ) between RT/CLK pin and GND determines the default switching frequency ( $f_{CLK}$ ).

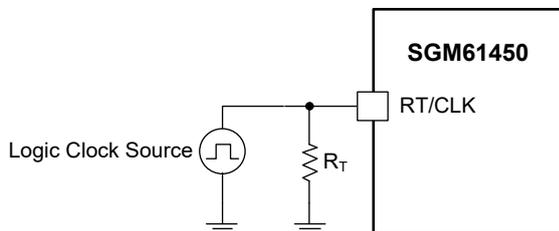


Figure 4. Synchronization to External Clock

### Low Dropout Operation and Bootstrap Voltage (BOOT Pin)

An internal regulator provides the bias voltage for gate driver using a 0.1μF ceramic capacitor. X5R or better dielectric types are recommended. The BOOT capacitor is refreshed when the high-side switch is off and the external low-side diode conducts.

The SGM61450 operates at maximum duty cycle when input voltage is closed to output voltage as long as the bootstrap voltage ( $V_{BOOT} - V_{SW}$ ) is greater than its UVLO threshold (2.6V). If the bootstrap voltage drops below 2.1V, the high-side switch will be temporarily turned off and an integrated small MOSFET at low-side will pull the SW voltage low to recharge  $C_{BOOT}$ . After the recharge, the high-side switch is turned on again to regulate the output. To reduce the losses of the integrated small low-side MOSFET at high output voltages, the function of  $C_{BOOT}$  refreshed is disabled when output voltage is over 24V and re-enabled when output voltage reaches 21.5V.

Because the small gate current sourced from  $C_{BOOT}$ , the high-side switch can remain on for many switching cycles before the switch is turned off to recharge the  $C_{BOOT}$ . Thus, this will effectively increase the SGM61450 switching duty cycle, approaching 100%.

### Internal Soft-Start

During each startup, a digital soft-start gradually ramps the regulation reference from 0V to 0.8V in 1365 switching cycles. The soft-start time is given in Equation 4.

$$t_{ss} \text{ (ms)} = \frac{1365}{f_{sw} \text{ (kHz)}} \quad (4)$$

Each time the SGM61450 is disabled, for example after a thermal shutdown or when the EN voltage falls below 1.18V, the device stops switching and resets the soft-start timer.

### Error Amplifier (EA)

This SGM61450 uses a transconductance amplifier to compare the sensed output voltage ( $V_{FB}$ ) and the internal reference as error amplifier (EA). The gain of EA amplifier in normal operation is 407μA/V. The output current is injected into the frequency compensation network (between COMP and GND pins) to produce the control signal ( $V_{COMP}$ ) for the PWM comparator.

## DETAILED DESCRIPTION (continued)

### Slope Compensation

Without implementing some slope compensation, the PWM pulse widths will be unstable and oscillatory at duty cycles above 50%. To avoid sub-harmonic oscillations in this device, an internal compensation ramp is added to the measured high-side switch current before comparing it with the control signal by the PWM comparator.

### Power-Save Mode

To reduce light load loss and increase the efficiency, power-save mode (PSM) feature is included in the SGM61450. When the peak inductor current is below PSM current threshold, the corresponding COMP pin voltage ( $V_{COMP}$ ) will be lower than 600mV. The device will enter PSM in such conditions.

In PSM,  $V_{COMP}$  is internally clamped at 600mV that inhibits the high-side MOSFET switching. The device can exit PSM if  $V_{COMP}$  rises above the clamp level and the peak inductor current exceeds current threshold. During PSM operation, the peak inductor current is the sensed parameter for entering the PSM, the actual load current (DC) threshold for PSM will depend on the output filter.

### Over-Current and Frequency Fold-Back Protections

Over-current protection (OCP) is naturally provided by current mode control. In each cycle, the high-side current sensing starts a short time (blanking time) after the high-side switch is turned on. The sensed high-side switch current is continuously compared with the current limit threshold and when the high-side current reaches to that threshold, the high-side switch is turned off. If the output is overloaded,  $V_{OUT}$  drops and  $V_{COMP}$  is increased by EA to compensate that. However, the EA output ( $V_{COMP}$ ) is clamped to a maximum value. By limiting the  $V_{COMP}$  (maximum peak current), the output current can actually be limited precisely.

The natural OCP of the peak current mode control may not be able to provide a complete protection when an output short-circuit occurs and an extra protection mechanism for short-circuit is needed. In a short-circuit event, the inductor current can significantly exceed the peak current limit threshold at high input voltage because the switch cannot be turned off as fast as needed due to the limited minimum on-time. During the output short, the inductor current decreases slowly because a small negative diode forward voltage appears across the inductor during the off-time, as a result the inductor current cannot be reset. In these conditions, current can saturate the inductor and the current may even increase higher until the device is damaged. In the SGM61450, this problem is effectively solved by increasing the off-time during short-circuit by reducing the switching frequency (frequency fold-back). As the output voltage drops and the FB pin voltage falls from 0.8V to 0V, the frequency will be divided by 1, 2, 4 and 8.

### Over-Voltage Protection

When an overload or an output fault condition is removed, large overshoots may occur on the output. The SGM61450 includes over-voltage protection (OVP) circuit to reduce such over-voltage transients. If the FB pin voltage exceeds 109% of the  $V_{REF}$  threshold, the high-side MOSFET is turned off. When it returns below 106% of the  $V_{REF}$  threshold, the high-side MOSFET is released again.

### Thermal Shutdown (TSD)

If the junction temperature ( $T_J$ ) exceeds +176°C, the TSD protection circuit will stop switching to protect the device from overheating. The device will automatically restart with a power up sequence when the junction temperature drops below +156°C.

APPLICATION INFORMATION

A typical application circuit for the SGM61450 as a Buck converter is shown in Figure 5. It is used for converting a 6V to 42V supply voltage to a lower voltage level supply voltage (3.3V) suitable for the system.

Typical Application

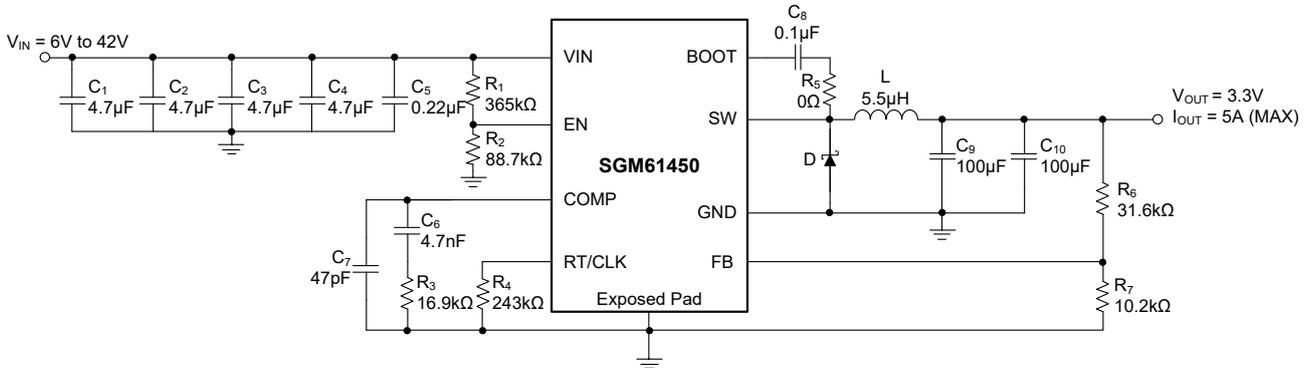


Figure 5. 3.3V Output SGM61450 Design Example

Design Requirements

The design parameters given in Table 1 are used for this design example.

Table 1. Design Parameters

Design Parameters	Example Values
Input Voltage	6V to 42V (12V TYP)
Start Input Voltage-Rising $V_{IN}$ ( $V_{START}$ )	5.55V
Stop Input Voltage-Falling $V_{IN}$ ( $V_{STOP}$ )	4.27V
Input Ripple Voltage	420mV
Output Voltage ( $V_{OUT}$ )	3.3V
Output Voltage Ripple ( $V_{RIPPLE}$ )	1% of $V_{OUT}$
Maximum Output Current ( $I_{OUT}$ )	5A
Transient Response ( $\Delta V_{OUT}$ ) 25% - 75% Load Steps	4%
Operation Frequency	420kHz

Switching Frequency Selection

Several parameters such as losses, inductor and capacitors sizes and response time are considered in selection of the switching frequency. Higher frequency increases the switching and gate charge losses. Lower frequency requires larger inductance and capacitances, and results in larger overall physical size and higher cost. Therefore, a tradeoff is needed between losses

and component size. If the application is noise-sensitive to a frequency range, the frequency should be selected out of that range.

For this design, a lower switching frequency of 420kHz is chosen and a 243kΩ resistor can be chosen for  $R_4$  according to Equation 3.

Input Capacitor Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61450. At least 3µF of effective capacitance (after deratings) is needed on the VIN input. In some applications additional bulk capacitance may also be required for the VIN input, for example, when the SGM61450 is more than 5cm away from the input source. The VIN capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 5 and the maximum value occurs at 50% duty cycle. Using the design example values,  $I_{OUT} = 5A$ , yields an RMS input ripple current of 2.5A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (5)$$

## APPLICATION INFORMATION (continued)

In this example, four 4.7µF/50V, X7R capacitors are used to cover capacitance deratings due to the operating DC voltage (42V MAX), aging and high ambient temperature. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 6. In this example, the total effective capacitance of the four 4.7µF/50V capacitors is around 7.4µF at 12V input, and the input voltage ripple is 420mV.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (6)$$

It is recommended to place an additional small size 0.22µF ceramic capacitor right beside VIN and GND pins (anode of the diode) for high frequency filtering.

### Inductor Design

Equation 7 is conventionally used to calculate the output inductance of a Buck converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple ( $\Delta I_L$ ) to the maximum output current ( $I_{OUT}$ ) is represented as  $K_{IND}$  factor ( $\Delta I_L/I_{OUT}$ ). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current ( $I_{OUT} + \Delta I_L/2$ ) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. The ripple current also affects the selection of the output capacitor.  $C_{OUT}$  RMS current rating must be higher than the inductor RMS ripple. Typically, a 20% to 40% ripple is selected ( $K_{IND} = 0.2 \sim 0.4$ ). Choosing a higher  $K_{IND}$  value reduces the selected inductance, but a too high  $K_{IND}$  factor may result in insufficient slope compensation.

$$L = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (7)$$

$K_{IND} = 0.3$  is a suitable choice when low-ESR ceramic capacitors are used for output capacitors.  $K_{IND} = 0.2$  is preferred when a high-ESR output capacitor is used. In this example, the calculated inductance will be 4.9µH with  $K_{IND} = 0.3$ , so the nearest larger inductance of 5.5µH is selected. The ripple, RMS and peak inductor current calculations are summarized in Equations 8, 9 and 10 respectively.

$$\Delta I_L = \frac{V_{IN\_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (8)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (9)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (10)$$

Note that during startup, load transients or fault conditions, the peak inductor current may exceed the calculated  $I_{L\_PEAK}$ . Therefore it is always safer to choose the inductor saturation current higher than the switch current limit.

### External Diode

An external power diode between the SW and GND pins is needed by the SGM61450 to complete the converter. This diode must tolerate the application's absolute maximum ratings. The reverse blocking voltage must be higher than  $V_{IN\_MAX}$  and its peak current must be above the maximum inductor current. Choose a diode with small forward voltage drop for higher efficiency. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 42V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SGM61450.

## APPLICATION INFORMATION (continued)

### Output Capacitor

Three primary criteria must be considered for design of the output capacitor ( $C_{OUT}$ ):

1. The converter pole location.
2. The output voltage ripple.
3. The transient response to a large change in load current.

The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of  $V_{OUT}$  in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 11 can be used to calculate the minimum output capacitance that is needed to supply a current step ( $\Delta I_{OUT}$ ) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of  $\Delta V_{OUT}$  (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (11)$$

where:

$\Delta I_{OUT}$  is the change in output current.

$\Delta V_{OUT}$  is the allowable change in the output voltage.

For example, if the acceptable transient from 1.25A to 3.75A load step is 4%, by inserting  $\Delta V_{OUT} = 0.04 \times 3.3V = 0.132V$  and  $\Delta I_{OUT} = 2.5A$ , the minimum required capacitance will be 95 $\mu$ F. Note that the impact of output capacitor ESR on the transient is not taken into account in Equation 11. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of  $\Delta V_{OUT}$  transient. However, for aluminum electrolytic and tantalum capacitors, or high current

power supplies, the ESR contribution to  $\Delta V_{OUT}$  must be considered.

When the load steps down, the excess inductor current will charge the capacitor and the output voltage will overshoot. The catch diode current cannot discharge  $C_{OUT}$ , so  $C_{OUT}$  must be large enough as given in Equation 12 to absorb the excess inductor energy with limited over-voltage. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 12 calculates the minimum capacitance required to keep the output-voltage overshoot to a desired value.

$$C_{OUT} > L \times \frac{I_{OUT\_H}^2 - I_{OUT\_L}^2}{(V_{OUT} + \Delta V_{OUT})^2 - V_{OUT}^2} \quad (12)$$

where:

$I_{OUT\_H}$  is the high level of the current step.

$I_{OUT\_L}$  is the low level of the current step.

For example, if the acceptable transient from 3.75A to 1.25A load step is 4%, by inserting  $\Delta V_{OUT} = 0.04 \times 3.3V = 0.132V$ , the minimum required capacitance will be 77.4 $\mu$ F.

Equation 13 can be used for the output ripple criteria and finding the minimum output capacitance needed.

$V_{OUT\_RIPPLE}$  is the maximum acceptable ripple. In this example, the allowed ripple is 33mV that results in minimum capacitance of 13.5 $\mu$ F.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (13)$$

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 13. For a specific output capacitance value, use Equation 14 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement.

$$ESR_{C_{OUT}} < \frac{V_{OUT\_RIPPLE}}{\Delta I_L} - \frac{1}{8 \times f_{SW} \times C_{OUT}} \quad (14)$$

## APPLICATION INFORMATION (continued)

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example,  $2 \times 100\mu\text{F}/10\text{V}$  X5R ceramic capacitors with  $2\text{m}\Omega$  of ESR are used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 15 calculates the RMS current that the output capacitor must support. In this example, it is  $380\text{mA}$ .

$$I_{\text{COUT\_RMS}} = \frac{V_{\text{OUT}} \times (V_{\text{IN\_MAX}} - V_{\text{OUT}})}{\sqrt{12} \times V_{\text{IN\_MAX}} \times L \times f_{\text{SW}}} \quad (15)$$

### Bootstrap Capacitor Selection

Use a  $0.1\mu\text{F}$  high-quality ceramic capacitor (X7R or X5R) with  $10\text{V}$  or higher voltage rating for the bootstrap capacitor ( $C_8$ ). A  $5\Omega$  to  $10\Omega$  resistor ( $R_5$ ) can be added in series with  $C_8$  to slow down switch-on speed of the high-side switch and reduce EMI if needed. Too high values for  $R_5$  may cause insufficient  $C_8$  charging in high duty-cycle applications. Slower switch-on speed will also increase switch losses and reduce efficiency.

### UVLO Setting

The input UVLO can be programmed using an external voltage divider on the EN pin of the device. In this example  $R_1$  is connected between VIN pin and EN pin and  $R_2$  is connected between EN and GND (see Figure 5). The turn-on (enable to start switching) occurs when  $V_{\text{IN}}$  rises above  $5.55\text{V}$  (UVLO rising threshold). When the regulator is working, it will not stop switching (disabled) until the input falls below  $4.27\text{V}$  (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are  $R_1 = 365\text{k}\Omega$  and  $R_2 = 88.7\text{k}\Omega$ .

### Feedback Resistors Setting

Use an external resistor divider ( $R_6$  and  $R_7$ ) to set the output voltage using Equations 16 and 17.

$$R_6 = R_7 \times \left( \frac{V_{\text{OUT}} - V_{\text{REF}}}{V_{\text{REF}}} \right) \quad (16)$$

$$V_{\text{OUT}} = V_{\text{REF}} \times \left( \frac{R_6}{R_7} + 1 \right) \quad (17)$$

In this example by selecting  $R_7 = 10.2\text{k}\Omega$  for the lower resistor, the calculated  $R_6$  value will be  $31.9\text{k}\Omega$  and a  $31.6\text{k}\Omega$  resistor is selected as the nearest standard 1% resistor.

### Compensation Network Setting

Several techniques are used by engineers to compensate a DC/DC regulator. The method presented here uses simple calculations and generally results in high phase margins. In most conditions, the phase margin will be between  $60$  and  $90$  degrees. In this method the effects of the slope compensation are ignored. Because of this approximation, the actual cross over frequency is usually lower than the calculated value.

First, the converter pole ( $f_p$ ) and ESR-zero ( $f_z$ ) are calculated from Equations 18 and 19. For  $C_{\text{OUT}}$ , the worst derated value of  $130\mu\text{F}$  should be used. Equations 20 and 21 can be used to find an estimation for closed-loop crossover frequency ( $f_{\text{CO}}$ ) as a starting point.

$$f_p = \frac{I_{\text{OUT}}}{2 \times \pi \times V_{\text{OUT}} \times C_{\text{OUT}}} \quad (18)$$

$$f_z = \frac{1}{2 \times \pi \times R_{\text{ESR}} \times C_{\text{OUT}}} \quad (19)$$

$$f_{\text{CO}} = \sqrt{f_p \times f_z} \quad (20)$$

$$f_{\text{CO}} = \sqrt{f_p \times \frac{f_{\text{SW}}}{2}} \quad (21)$$

For this design,  $f_p = 1.85\text{kHz}$  and  $f_z = 610\text{kHz}$ . Equation 20 yields  $33.6\text{kHz}$  and Equation 21 gives  $19.2\text{kHz}$ . Use the geometric mean value of Equation 20 and Equation 21 for an initial crossover frequency. In this application example, the lab experiments shows that to achieve the required transient response the crossover frequency must be at least  $f_{\text{CO}} = 30\text{kHz}$ . Having the crossover frequency, the compensation network ( $R_3$  and  $C_6$ ) can be calculated.  $R_3$  sets the gain of the compensated network at the crossover frequency and can be calculated by Equation 22.

$$R_3 = \frac{2 \times \pi \times f_{\text{CO}} \times C_{\text{OUT}} \times V_{\text{OUT}}}{g_m \times V_{\text{REF}} \times g_{\text{mps}}} \quad (22)$$

**APPLICATION INFORMATION (continued)**

C<sub>6</sub> sets the location of the compensation zero along with R<sub>3</sub>. To place this zero on the converter pole, use Equation 23

$$C_6 = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_3} \tag{23}$$

From Equations 22 and 23 the standard selected values are R<sub>3</sub> = 16.9kΩ and C<sub>6</sub> = 4.7nF.

If needed, a far compensation pole can be added by adding capacitor C<sub>7</sub> to further reduce high frequency loop gain for better transient stability. The larger value between the two values calculated from Equations 24 and 25 can be used for C<sub>7</sub>. In this example C<sub>7</sub> = 47pF is selected.

$$C_7 = \frac{C_{OUT} \times R_{ESR}}{R_3} \tag{24}$$

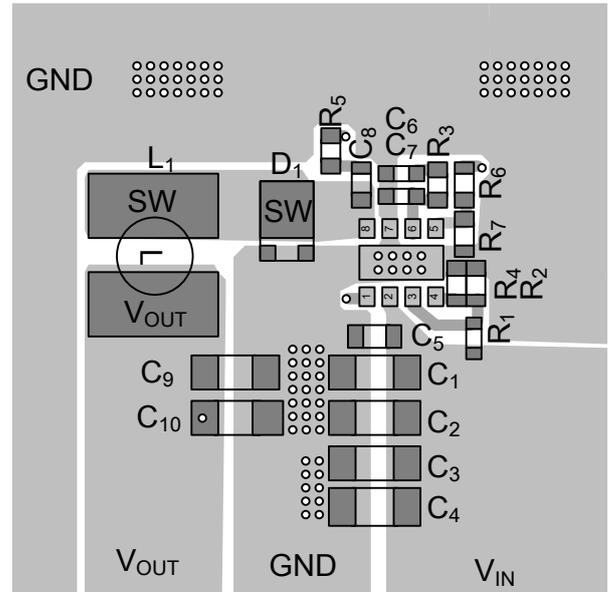
$$C_7 = \frac{1}{R_3 \times f_{SW} \times \pi} \tag{25}$$

**Layout Considerations**

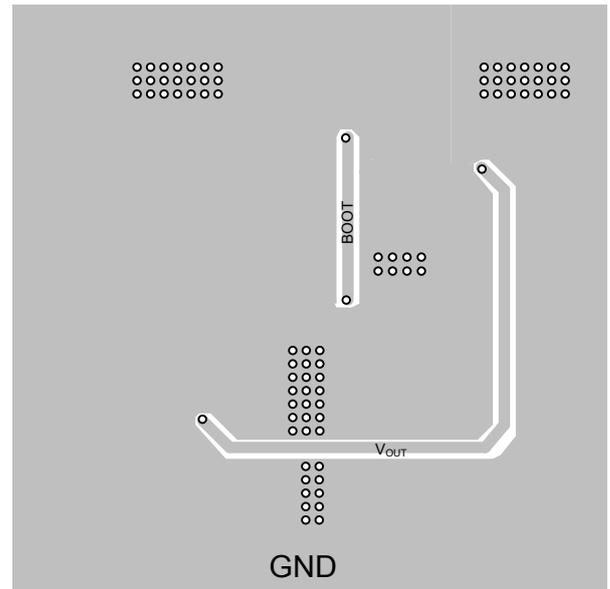
PCB layout is an important part of the converter design. A weak layout can result in poor performance, resistive losses, EMI issues and instability problems. The following guidelines are helpful for designing a good layout for the SGM61450.

- ◆ Bypass the VIN pin to GND pin (where it connects to the anode pin of the power diode) with low-ESR ceramic capacitors and place them as close as possible to the device.
- ◆ Connect the diode as close as possible to SW and GND pins.
- ◆ Share the same GND connection point with the input and output capacitors.
- ◆ Connect the device GND to the PCB ground plane right at the GND pin.
- ◆ Stitch the exposed pad to the internal ground planes and the back side of the PCB directly under the IC using multiple thermal vias.
- ◆ Minimize the length and the area of the connection route from SW pin to the cathode of the diode and the inductor to reduce the noise coupling from this area.
- ◆ Minimize FB trace length and keep both feedback resistors close to the FB pin. Bring the V<sub>OUT</sub> sense trace from the point where V<sub>OUT</sub> accuracy is important and keep it away from the noisy nodes (SW), preferably through another layer that is on the other side of a shield layer.

- ◆ Place the R<sub>T</sub> resistor as close as possible to the RT/CLK pin with short routes.
- ◆ Choose wide traces for V<sub>IN</sub>, V<sub>OUT</sub> and ground to minimize voltage drops and maximize efficiency.
- ◆ For operation at full-rated load, the top side ground area must provide adequate heat dissipating area.



**Top Layer**



**Bottom Layer**

**Figure 6. Layout**

**REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>FEBRUARY 2023 – REV.A to REV.A.2</b>	<b>Page</b>
Updated Electrical Characteristics .....	4

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<b>OCTOBER 2022 – REV.A to REV.A.1</b>	<b>Page</b>
Updated Layout Considerations.....	18

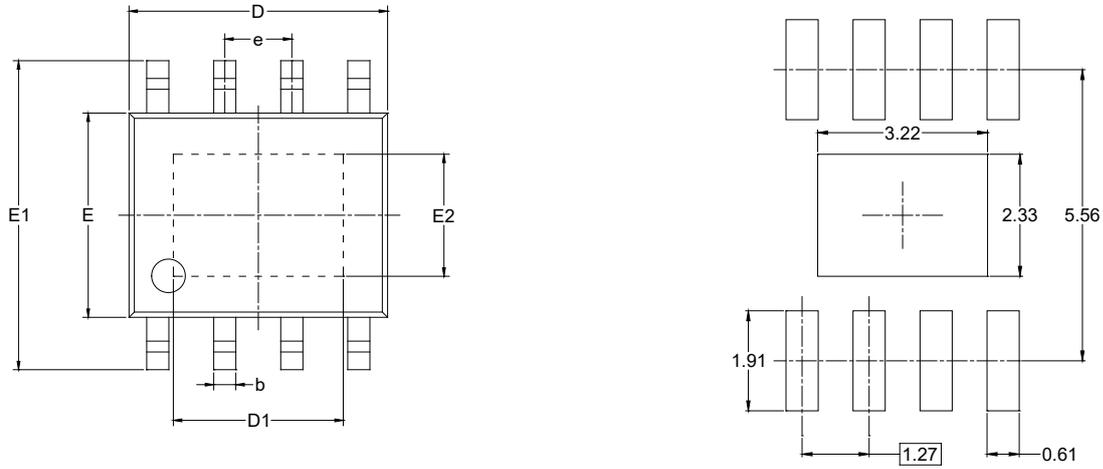
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<b>Changes from Original (MARCH 2022) to REV.A</b>	<b>Page</b>
Changed from product preview to production data.....	All

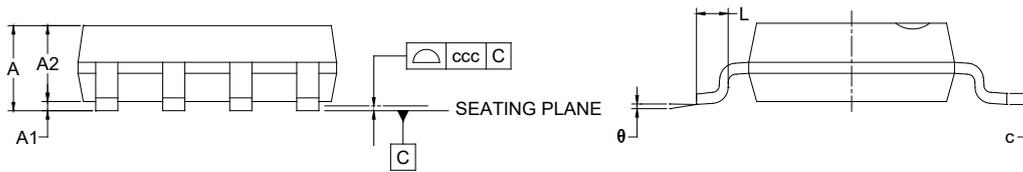
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PACKAGE OUTLINE DIMENSIONS

SOIC-8 (Exposed Pad)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

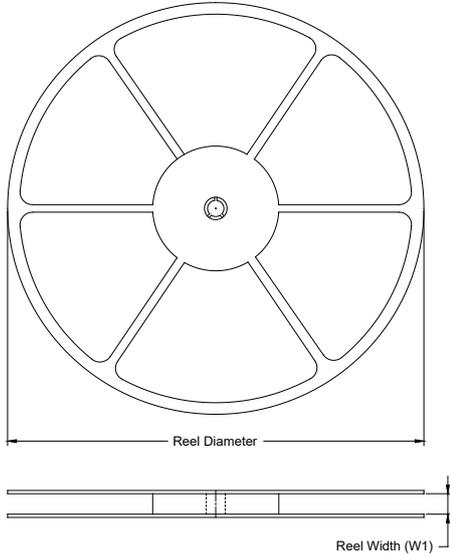
NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

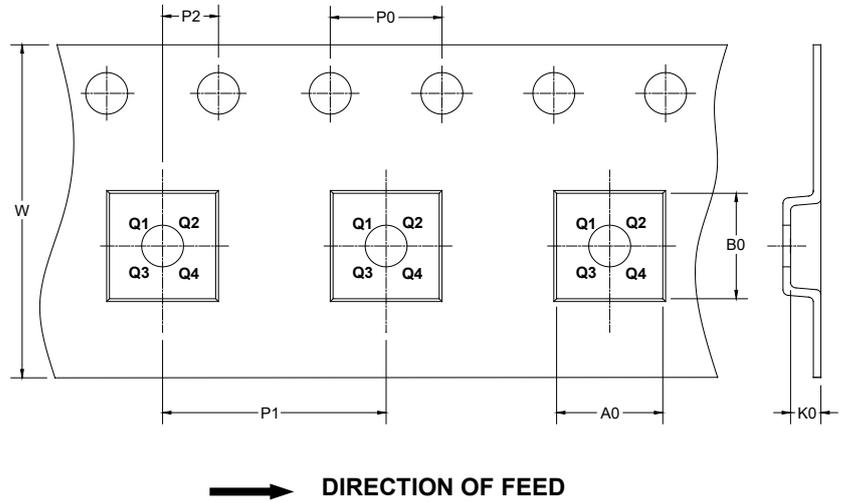
# PACKAGE INFORMATION

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

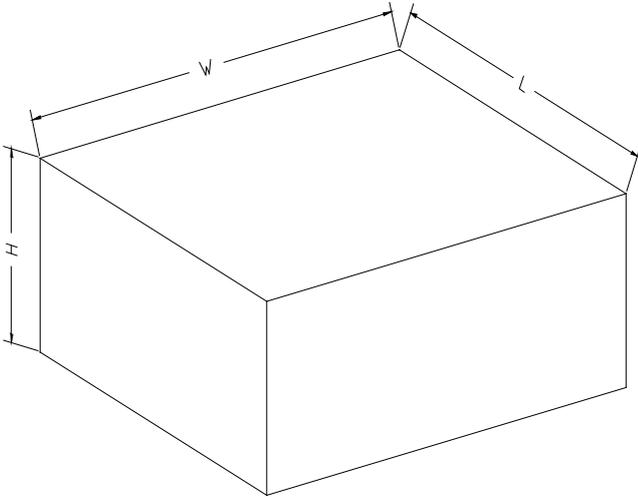
### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

000001

# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002