SGM42553
3A Triple Half-Bridge Motor Driver

GENERAL DESCRIPTION

The SGM42553 is a triple half-bridge driver, and each channel is controlled by separate controllable input. This device is designed to drive a three-phase brushless DC motor, as well as solenoids or other loads. The output driver block for each consists of N-MOSFETs configured as half-bridge to drive the motor. This device integrates three dedicated ground terminals (PGNDx) for each channel to sense the external current independently.

The SGM42553 integrates a comparator, which can be used if current limit function is needed in the motor system.

A number of protection features are provided in the device including under-voltage lockout, short-circuit, over-current and over-temperature shutdown. The nFAULT pin is used to indicate the fault problems.

The SGM42553 is available in a Green TSSOP-28 (Exposed Pad) package.

FEATURES

- **Motor Supply Voltage Range: 8V to 45V**
- **Three Half-Bridges**
- **High Output Current Capability: 3A Peak**
- **Low On-Resistance**
- **Individual Controllable Input**
- **Built-in Comparator**
- **Built-in LDO Regulator: 3.3V/10mA**
- **Low Power Sleep Mode**
- **Available in a Green TSSOP-28 (Exposed Pad) Package**

APPLICATIONS

Communication Systems
Gimbals

SIMPLIFIED SCHEMATIC

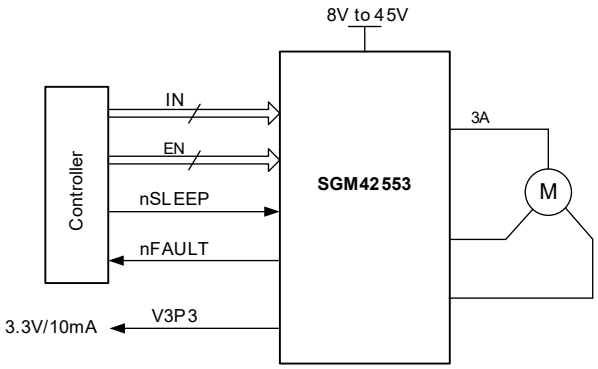


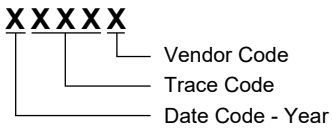
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42553	TSSOP-28 (Exposed Pad)	-40℃ to +125℃	SGM42553XPTS28G/TR	SGM42553 XPTS28 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_M ..... -0.3V to 50V
Power Supply Voltage Ramp Rate, V_M 2V/μs
Charge Pump Voltage, VCP, CPH..... -0.3V to V_M + 4.5V
Charge Pump Negative Switching Pin, CPL ..... -0.3V to V_M
Internal Regulator Current Output, V3P3 ..... 10mA
Internal Regulator Voltage, V3P3 ..... -0.3V to 3.8V
Control Pin Voltage, nRESET, nSLEEP, nFAULT, nCOMPO, ENx, INx..... -0.5V to 6V
Comparator Input-Voltage, COMPP, COMPN ..... -0.5V to 6V
Open-Drain Output Current, nFAULT, nCOMPO 10mA
Continuous Phase Node Pin Voltage, OUTx ..... -0.5V to V_M + 0.5V
Continuous Half-Bridge Source Voltage, PGNDx ..... -600mV to 600mV
Peak Output Current, OUTx..... Internally Limited
Package Thermal Resistance
TSSOP-28 (Exposed Pad), θ_{JA} ..... 28℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage, V_M .....8V to 45V
Digital Pin Voltage, V_{IN}.....0V to 5.5V
Applied PWM Signal on ENx, INx, f_{PWM} 250kHz
PGNDx Pin Voltage, V_{GNDX}.....-500mV to 500mV
V3P3 Load Current, I_{V3P3}..... 10mA

NOTE: 1. V_{CLAMP} is only used to supply the clamp diodes. It is not a power supply input.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

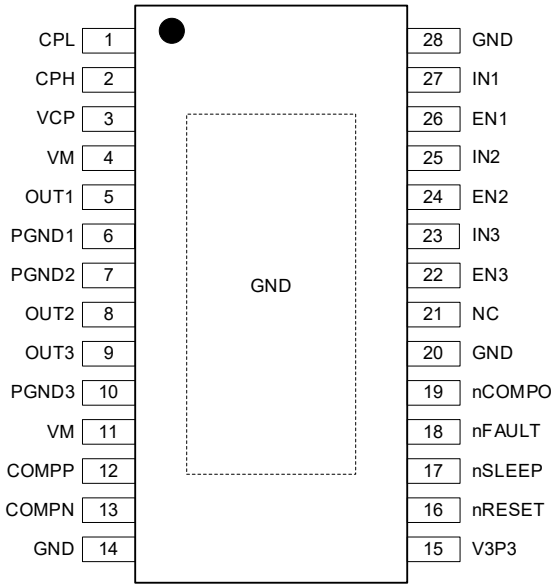
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM42553 (TOP VIEW)



TSSOP-28 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	CPL	P	Charge Pump Flying Capacitor. A 0.01μF capacitor is used between CPH and CPL pins.
2	CPH	P	
3	VCP	P	Gate Drive Voltage. Decouple with a 0.1μF/16V ceramic capacitor to VM pin.
4, 11	VM	P	Power Supply. Connect these pins to the motor supply (8V to 45V) and bypass each with a 0.1μF ceramic capacitor to GND. Connect sufficient bulk capacitance to the common supply line.
5	OUT1	O	Output of the Device.
8	OUT2	O	
9	OUT3	O	
6	PGND1	P	The Source Pin of Low-side MOSFET. If current sense is needed, connect the sense resistor to GND; if not, short it to GND directly.
7	PGND2	P	
10	PGND3	P	
12	COMPP	I	Positive Input of the Uncommitted Comparator.
13	COMPN	I	Negative Input of the Uncommitted Comparator.
14, 20, 28	GND	P	Ground.
15	V3P3	P	3.3V Regulator Output. A 0.47μF/6.3V ceramic capacitor is used between V3P3 and GND pins.
16	nRESET	I	Reset Input. Active-low reset input with weak internal pull-down initializes internal logic and disables half-bridge outputs.
17	nSLEEP	I	Sleep Mode Input. Active-low sleep mode logic input with weak internal pull-down. Apply high to enable device, and low to enter into the low power sleep mode.
18	nFAULT	OD	Fault Indication Pin. Open-drain output type, logic low when in fault conditions.
19	nCOMPO	OD	Output of the Uncommitted Comparator. Open-drain output type with external pull-up.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
21	NC	-	No Connection.
22	EN3	I	Enable Input for Each Channel. Active-high enable logic input with weak internal pull-down.
24	EN2	I	
26	EN1	I	
27	IN1	I	Logic Input for Each Channel. When ENx is high, logic high to turn on high-side MOSFET, and logic low to turn on low-side MOSFET.
25	IN2	I	
23	IN3	I	
GND	Exposed Pad	P	Ground.

NOTE: I = input, O = output, OD = open-drain output, P = power.

ELECTRICAL CHARACTERISTICS

(T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supplies						
Operating Supply Current	I_{VM}	V_M = 24V, f_{PWM} < 50kHz		0.8	3	mA
Sleep Mode Supply Current	I_{VMQ}	V_M = 24V		350	800	μA
Internal Regulator (V3P3)						
V3P3 Voltage	V_{3P3}	I_{OUT} = 0mA to 10mA	3.1	3.3	3.52	V
Logic-Level Inputs (nSLEEP, ENx, INx)						
Input Low Voltage	V_{IL}	T_J = -40℃ to +125℃			0.6	V
Input High Voltage	V_{IH}	T_J = -40℃ to +125℃	1.7			V
Input Hysteresis	V_{HYS}		50		400	mV
Input Low Current	I_{IL}	V_{IN} = 0V	-5		5	μA
Input High Current	I_{IH}	V_{IN} = 3.3V			100	μA
Pull-Down Resistance	R_{PD}			250		kΩ
Open-Drain Outputs (nFAULT and nCOMPO)						
Output Low Voltage	V_{OL}	I_O = 5mA			0.6	V
Output High Leakage Current	I_{OH}	V_O = 3.3V			1	μA
Comparator (COMPP, COMPN, nCOMPO)						
Input Common Mode Voltage Range	V_{CM}		0		5	V
Input Offset Voltage	V_{IO}		-18		18	mV
Input Bias Current	I_{IB}		-1		1	μA
Response Time	t_R	100mV step with 10mV overdrive		0.43		μs
Half-Bridge FETs						
High-side FET On-Resistance	R_{DSON}	V_M = 24V, I_O = 0.5A, T_J = +25℃		0.18		Ω
		V_M = 24V, I_O = 0.5A, T_J = +85℃		0.22	0.32	
Low-side FET On-Resistance		V_M = 24V, I_O = 0.5A, T_J = +25℃		0.18		Ω
		V_M = 24V, I_O = 0.5A, T_J = +85℃		0.22	0.32	
Protection Circuits						
VM Under-Voltage Lockout Voltage	V_{UVLO}	V_M rising		6.5	7.5	V
Over-Current Protection Trip Level	I_{OCP}			3		A
Over-Current Protection Deglitch Time	t_{OCP}			4		μs
Thermal Shutdown Temperature	T_{SD}	Die temperature		160		℃
Thermal Shutdown Hysteresis	T_{HYS}	Die temperature		20		℃

TIMING REQUIREMENTS

(T_J = +25℃, V_M = 24V, R_L = 50Ω, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delay Time 1	t_1	ENx high to OUTx high, INx = 1	40		250	ns
Delay Time 2	t_2	ENx low to OUTx low, INx = 1	120		420	ns
Delay Time 3	t_3	ENx high to OUTx low, INx = 0	110		310	ns
Delay Time 4	t_4	ENx low to OUTx high, INx = 0	120		330	ns
Delay Time 5	t_5	INx high to OUTx high, ENx = 1	210		500	ns
Delay Time 6	t_6	INx low to OUTx low, ENx = 1	110		420	ns
Output Rise Time	t_R	Resistive to GND	25		130	ns
Output Fall Time	t_F	Resistive to GND	25		130	ns
Output Dead Time	t_{DEAD}			90		ns

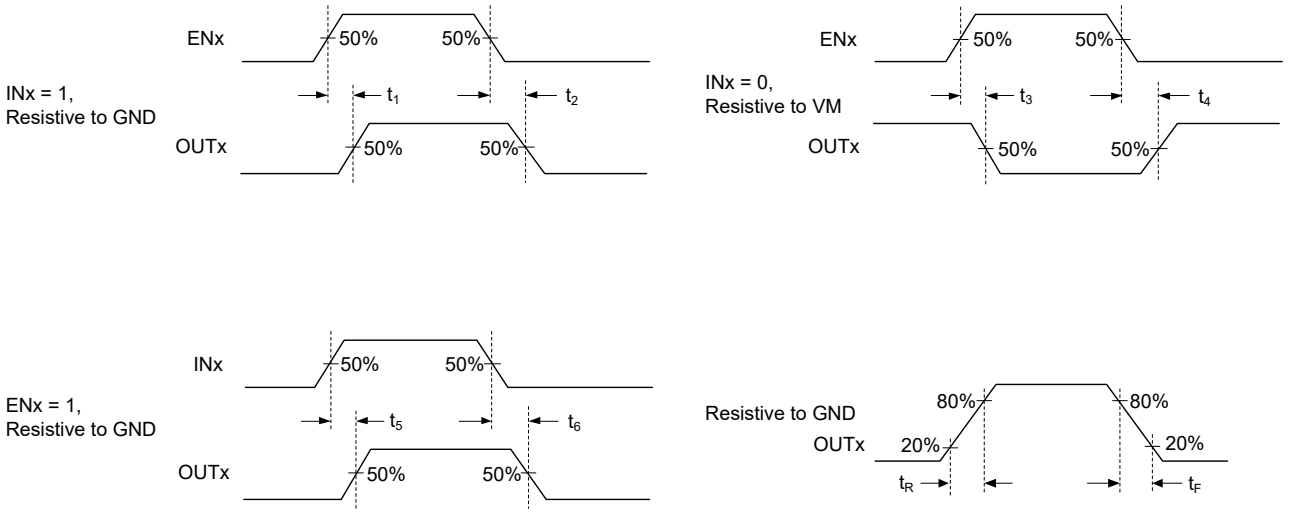
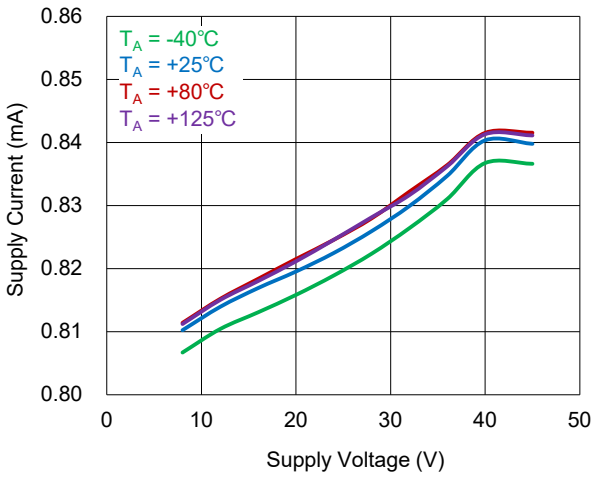


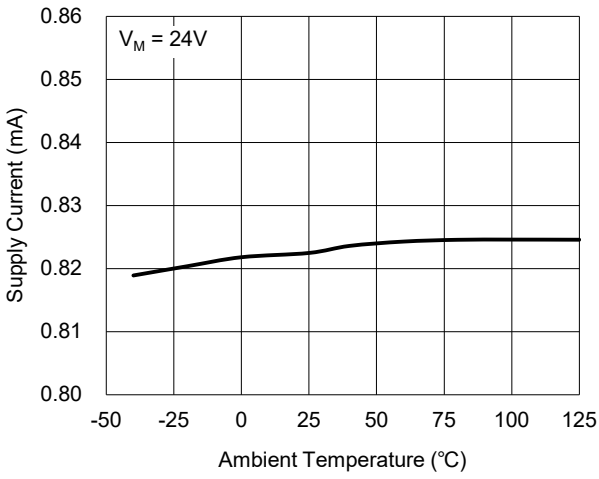
Figure 2. SGM42553 Timing Definitions

TYPICAL PERFORMANCE CHARACTERISTICS

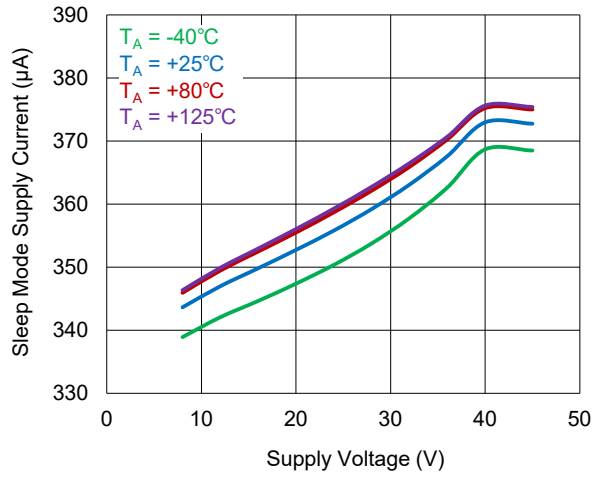
Supply Current vs. Supply Voltage



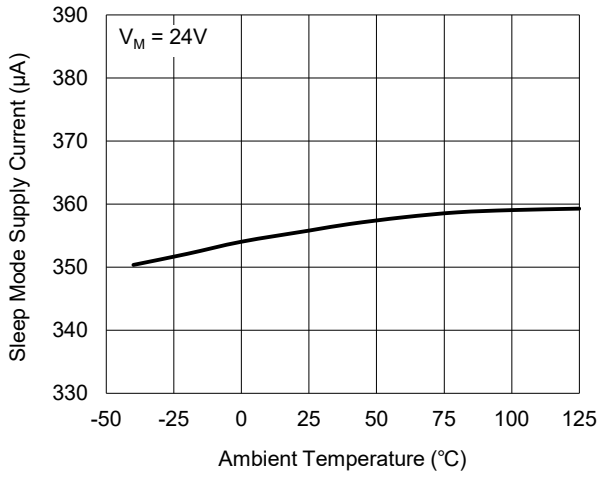
Supply Current vs. Ambient Temperature



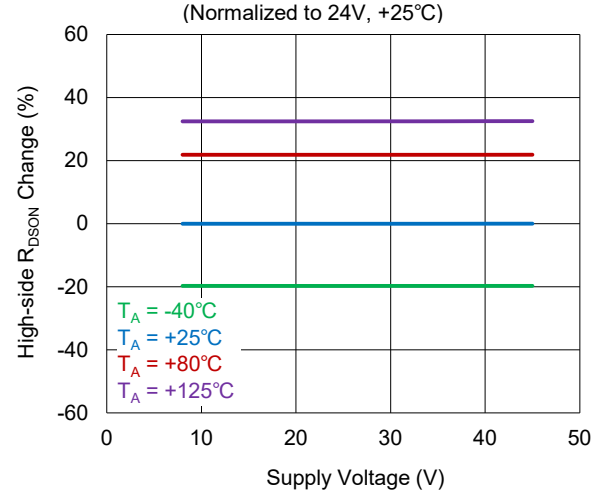
Sleep Mode Supply Current vs. Supply Voltage



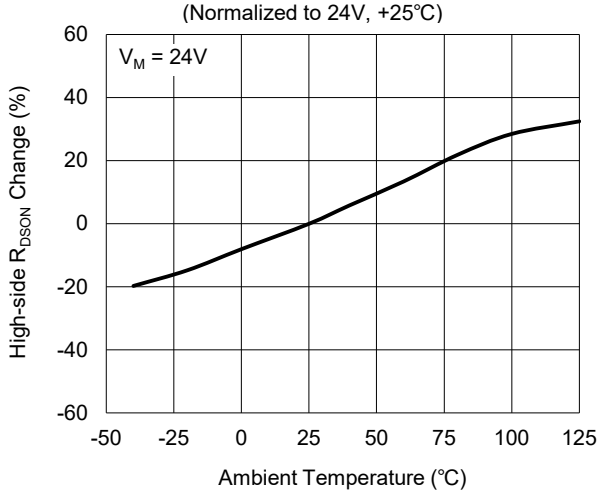
Sleep Mode Supply Current vs. Ambient Temperature



High-side R_{DSON} Change vs. Supply Voltage
(Normalized to 24V, +25℃)

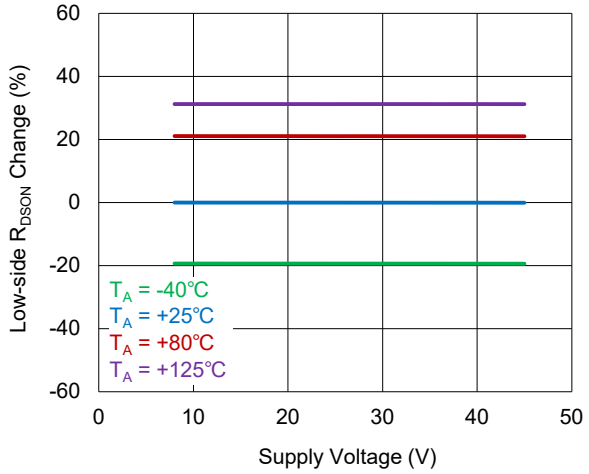


High-side R_{DSON} Change vs. Ambient Temperature
(Normalized to 24V, +25℃)

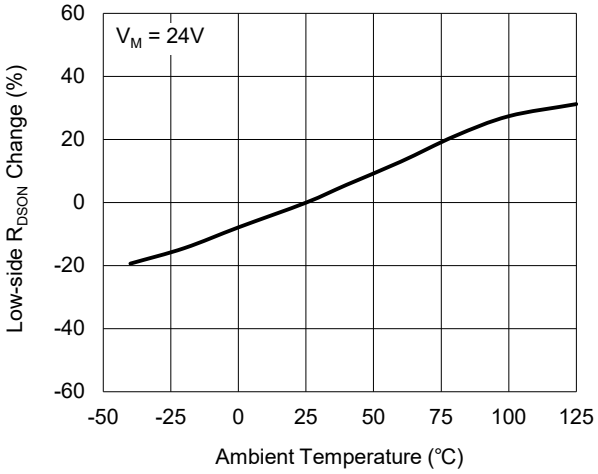


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

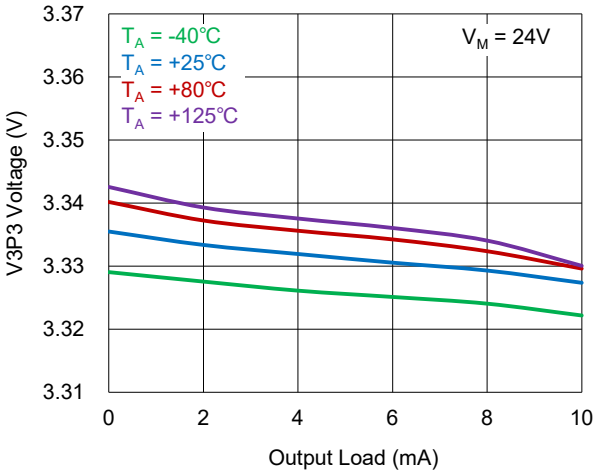
Low-side R_{DSON} Change vs. Supply Voltage
(Normalized to 24V, +25℃)



Low-side R_{DSON} Change vs. Ambient Temperature
(Normalized to 24V, +25℃)



V3P3 Voltage vs. Output Load



TYPICAL APPLICATION CIRCUIT

Please refer to the SGM42553 application circuit below, which is used in a BLDC control system.

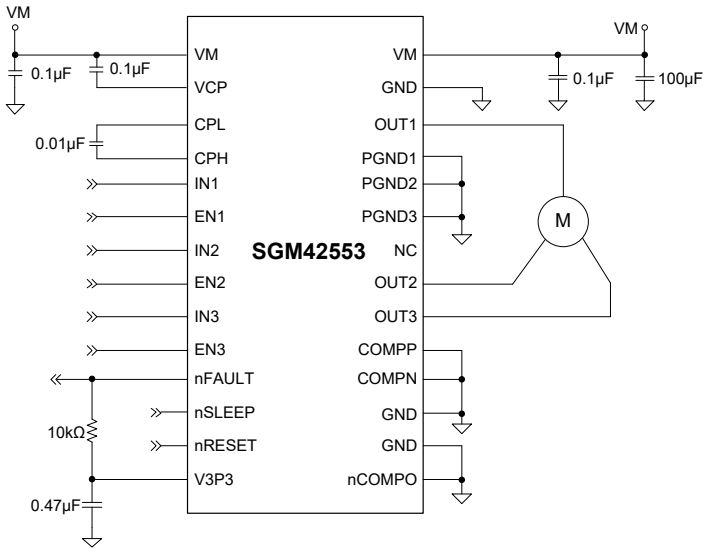


Figure 3. BLDC Driver Application Circuit

Motor Commutation

The SGM42553 can be used in trapezoidal or sinusoidal BLDC control system, depending on the micro-controller algorithm and PWM input.

Table 1. Trapezoidal (120°) Commutation States

State	OUT1 (Phase U)			OUT2 (Phase V)			OUT3 (Phase W)		
	IN1	EN1	OUT1	IN2	EN2	OUT2	IN3	EN3	OUT3
1	X	0	Hi-Z	1	1	H	0	1	L
2	1	1	H	X	0	Hi-Z	0	1	L
3	1	1	H	0	1	L	X	0	Hi-Z
4	X	0	Hi-Z	0	1	L	1	1	H
5	0	1	L	X	0	Hi-Z	1	1	H
6	0	1	L	1	1	H	X	0	Hi-Z
Brake	0	1	L	0	1	L	0	1	L
Coast	X	0	Hi-Z	X	0	Hi-Z	X	0	Hi-Z

FUNCTIONAL BLOCK DIAGRAM

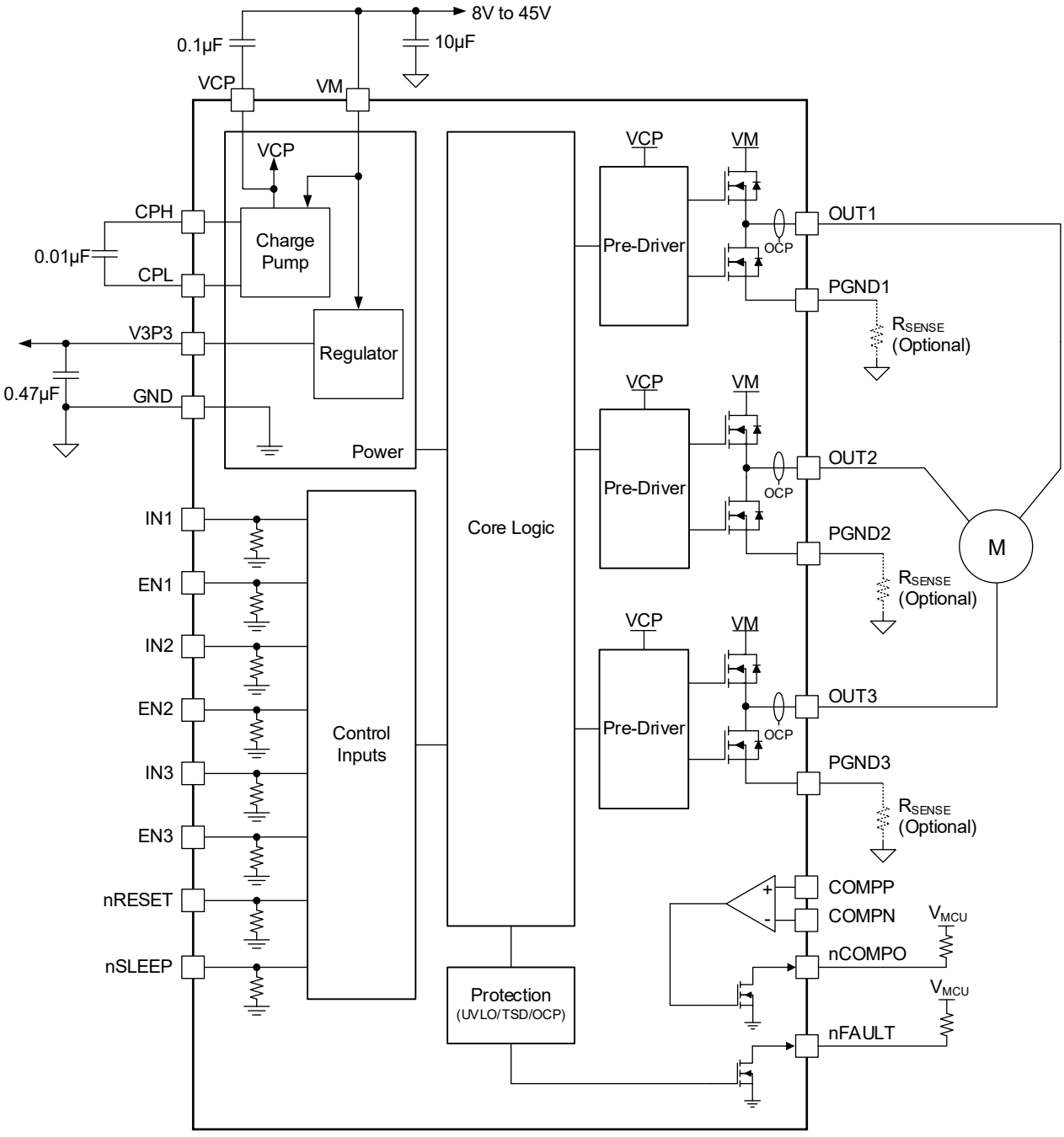


Figure 4. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM42553 provides three 3A half-bridge drivers, each channel is controlled by separate controllable input. It is suitable for driving brushless DC motors, brushed DC motors, and solenoid loads. The device is allowed to operate from a wide power supply of 8V to 45V.

Bridge Control

Please refer to the INx control logic in Table 2.

Table 2. Logic States

INx	ENx	OUTx
X	0	Hi-Z
0	1	L
1	1	H

Charge Pump

A charge pump is used to generate the gate drive for the high-side FETs. Two external capacitors are needed for the charge pump, one between VM and VCP pins and one between CPL and CPH pins. As the nSLEEP is pulled low, the charge pump will be turned off. See the following figure for details.

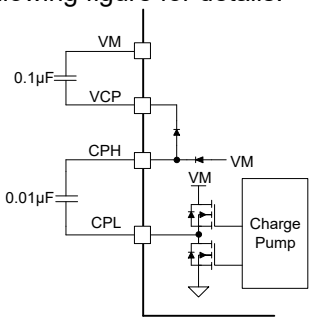


Figure 5. SGM42553 Charge Pump

Comparator

The SGM42553 integrates a comparator inside the device, which is commonly used as current limit detection. Please refer to the diagram below in Figure 6, which is the typical application circuit for current limit function.

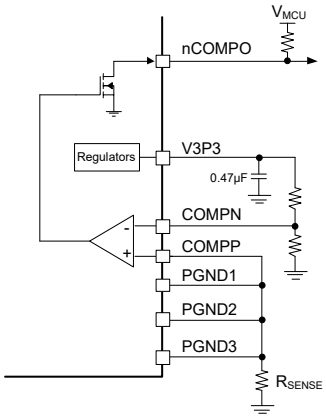


Figure 6. Comparator as Current Monitor

Protection Circuits

The SGM42553 integrated internal circuit protections include thermal shutdown, under-voltage lockout (UVLO), and over-current protection.

Under-Voltage Lockout (UVLO)

If the voltages on VM pin fall below their under-voltage lockout thresholds, the device will be disabled, charge pump will be turned off, and internal logic will be reset. Device resumes operation when all of them go back above their UVLO thresholds. When under-voltage locking occurs, the nFAULT is pulled down, after the device returns to work, the nFAULT is released.

Thermal Shutdown (TSD)

All bridges and drivers are shutdown if a junction over-temperature occurs in the device and the nFAULT pin will be driven low. Once the temperature goes back to the safe level, device resumes its operation.

Over-Current Protection (OCP)

Each MOSFET is protected by its own over-current protection circuit. In case of an over-current (any direction), only the specific half-bridge may be turned off, the nFAULT pin will be driven low. An over-current will occur due to a short between a switching node and ground or to the VM supply line, or to the other node of the bridge (a winding short).

Table 3. Fault Condition Summary

Fault	Condition	Error Report	H-Bridge	Charge Pump	V3P3	Recovery
VM Under-Voltage (UVLO)	$V_M < V_{UVLO}$	nFAULT	Disabled	Disabled	Operating	$V_M > V_{UVLO}$
Thermal Shutdown (TSD)	$T_J > T_{SD}$	nFAULT	Disabled	Operating	Operating	$T_J < T_{SD} - T_{HYS}$
Over-Current Protection (OCP)	$I_{OUT} > I_{OCP}$	nFAULT	Disabled	Operating	Operating	nRESET

DETAILED DESCRIPTION (continued)

Output Stage

If current sensing is needed in the motor control system, it is needed to connect the sense resistor from PGNDx to GND. When choosing the sense resistor, make sure that the PGNDx voltage is below ±500mV, and the package of the sense resistor can stand the power dissipation (I^2 × R). Low inductance resistor is recommended, and the resistor should be placed close to the PGNDx pin on the PCB layout.

Functional Modes

To idle the device and put it in the low power sleep mode, the nSLEEP pin can be pulled low. In the sleep mode, all half-bridges are disabled, internal clocks are paused, and the charge pumps for the gate drivers are stopped. All logic inputs are ignored in sleep mode.

nRESET and nSLEEP Operation

When the nRESET pin is pulled low, the half-bridges are all disabled. The nRESET is an active-low reset input for the internal logic. All other logic inputs are ignored if nRESET is low.

The nSLEEP is an active-low input to put the device in low power (sleep mode) state. In sleep mode, all internal clocks, bridges, charge pump are disabled. All logic inputs are ignored. V3P3 regulator stays on when device is in sleep mode. When waking up from sleep mode, time delay (about 1ms) is needed before outputs operate.

Table 4. Functional Modes Summary

Fault	Condition	H-Bridge	Charge Pump	V3P3
Operating	8V < V_M < 45V nSLEEP pin = high	Operating	Operating	Operating
Sleep Mode	8V < V_M < 45V nSLEEP pin = low	Disabled	Disabled	Operating
Fault Encountered	V_M Under-Voltage (UVLO)	Disabled	Disabled	Operating
	Over-Current Protection (OCP)	Disabled	Operating	Operating
	Thermal Shutdown (TSD)	Disabled	Operating	Operating

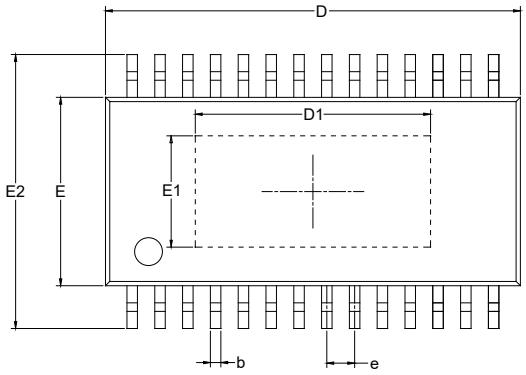
REVISION HISTORY

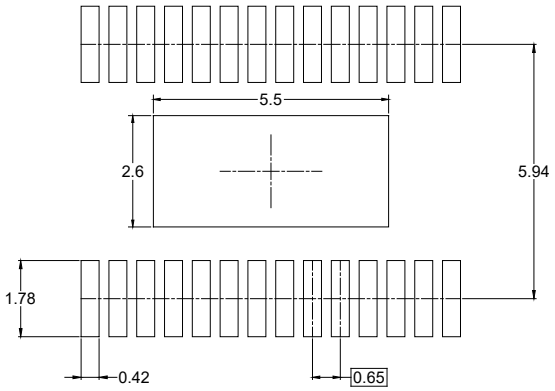
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

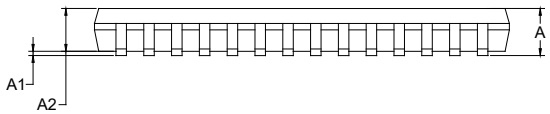
PACKAGE OUTLINE DIMENSIONS

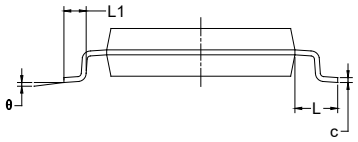
TSSOP-28 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





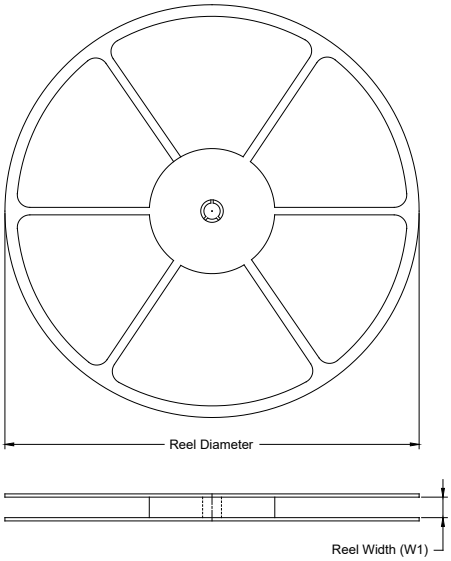
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	5.300	5.700	0.209	0.224
E	4.300	4.500	0.169	0.177
E1	2.400	2.800	0.094	0.110
E2	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	1.000 BSC		0.039 BSC	
L1	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

NOTES:

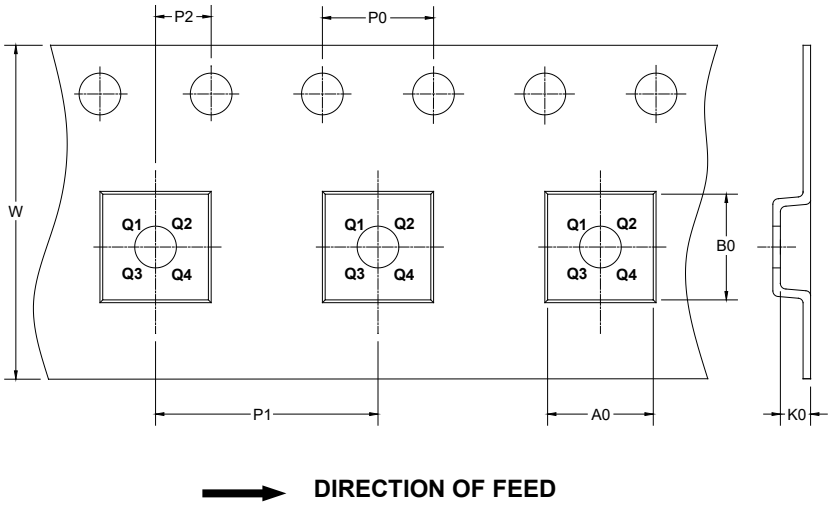
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

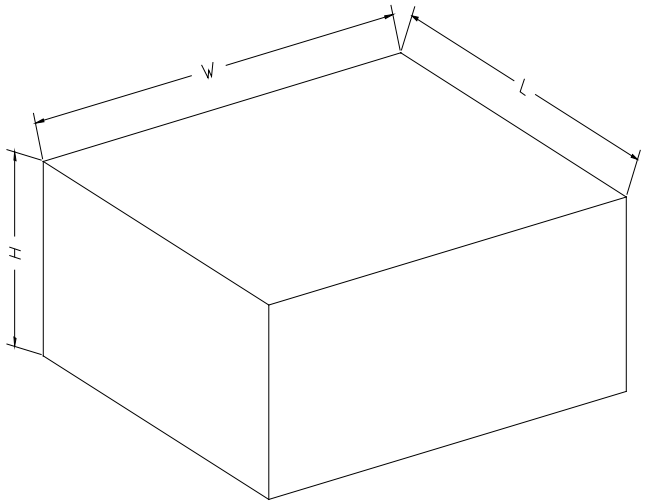
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-28 (Exposed Pad)	13″	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002